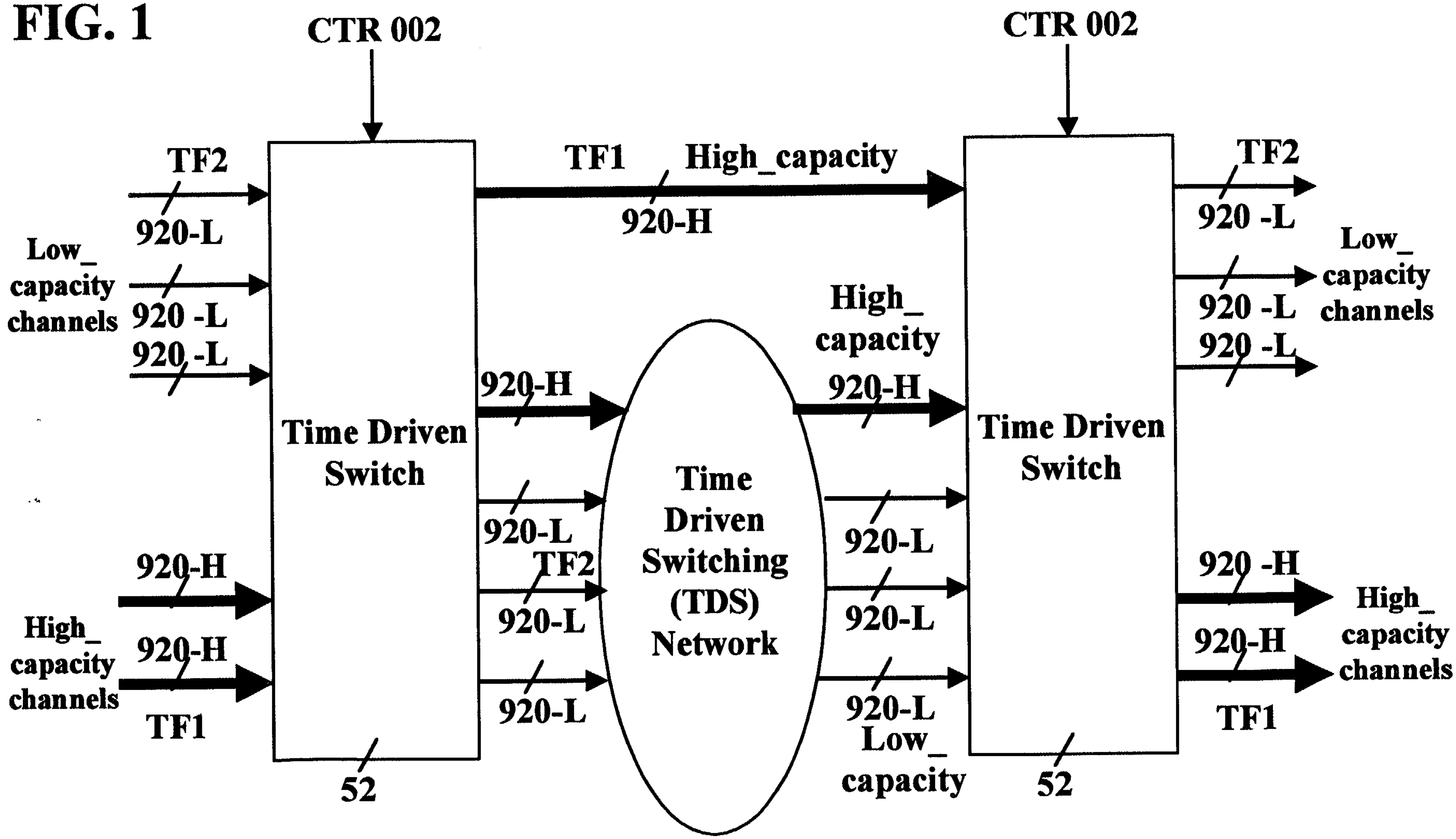
FIG. 1



c = High_capacity/Low_capacity

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FIG. 2

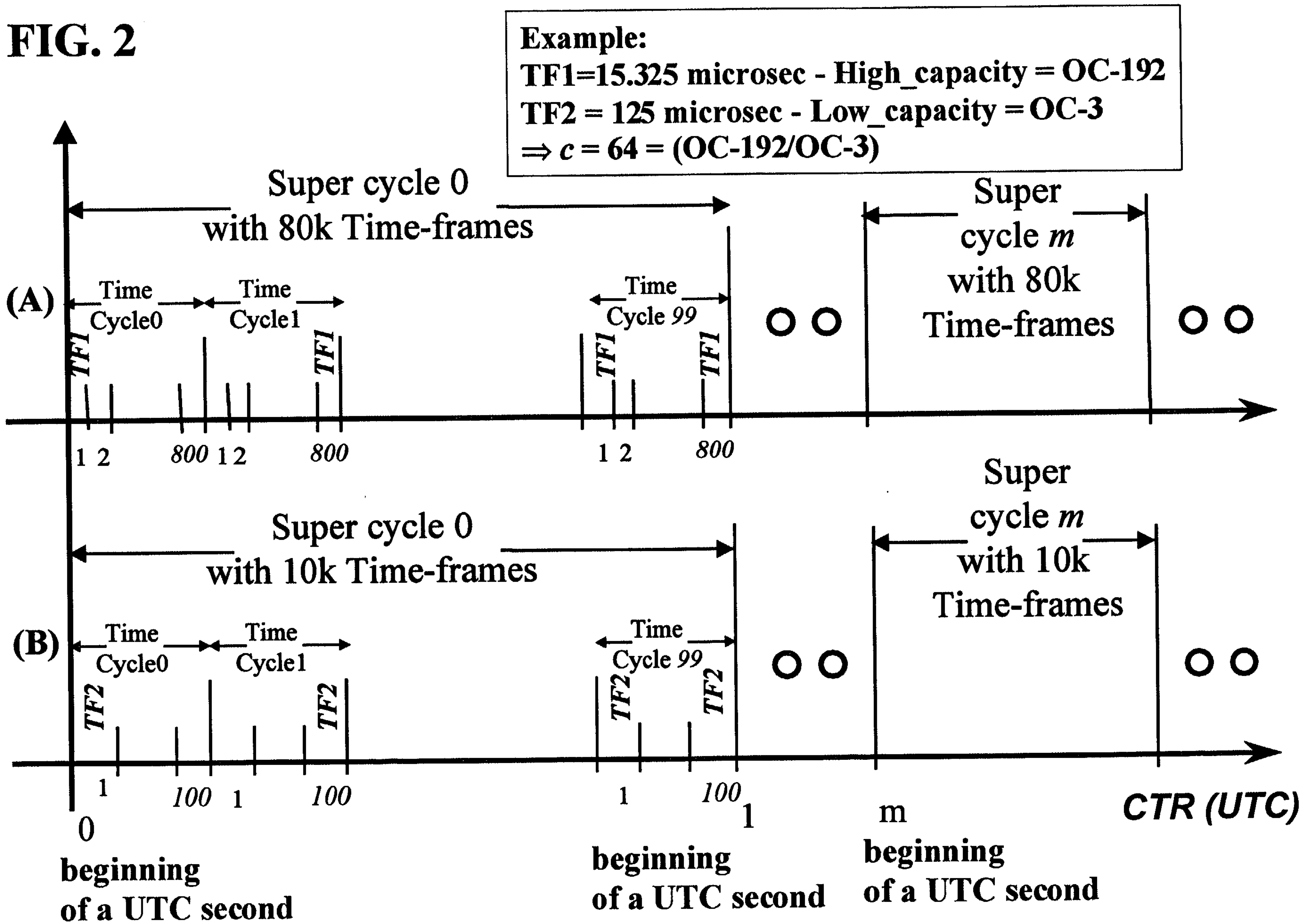

Example:
TF1=15.325 microsec - High_capacity = OC-192
TF2 = 125 microsec - Low_capacity = OC-3
⇒ c = 64 = (OC-192/OC-3)
Super cycle 0 with 80k Time-frames
Super cycle m with 80k Time-frames
(A)
Time Cycle0
Time Cycle1
Time Cycle 99
TF1
1 2
800
Super cycle 0 with 10k Time-frames
Super cycle m with 10k Time-frames
(B)
TF2
1
100
0
1
m
CTR (UTC)
beginning of a UTC second

FIG. 3

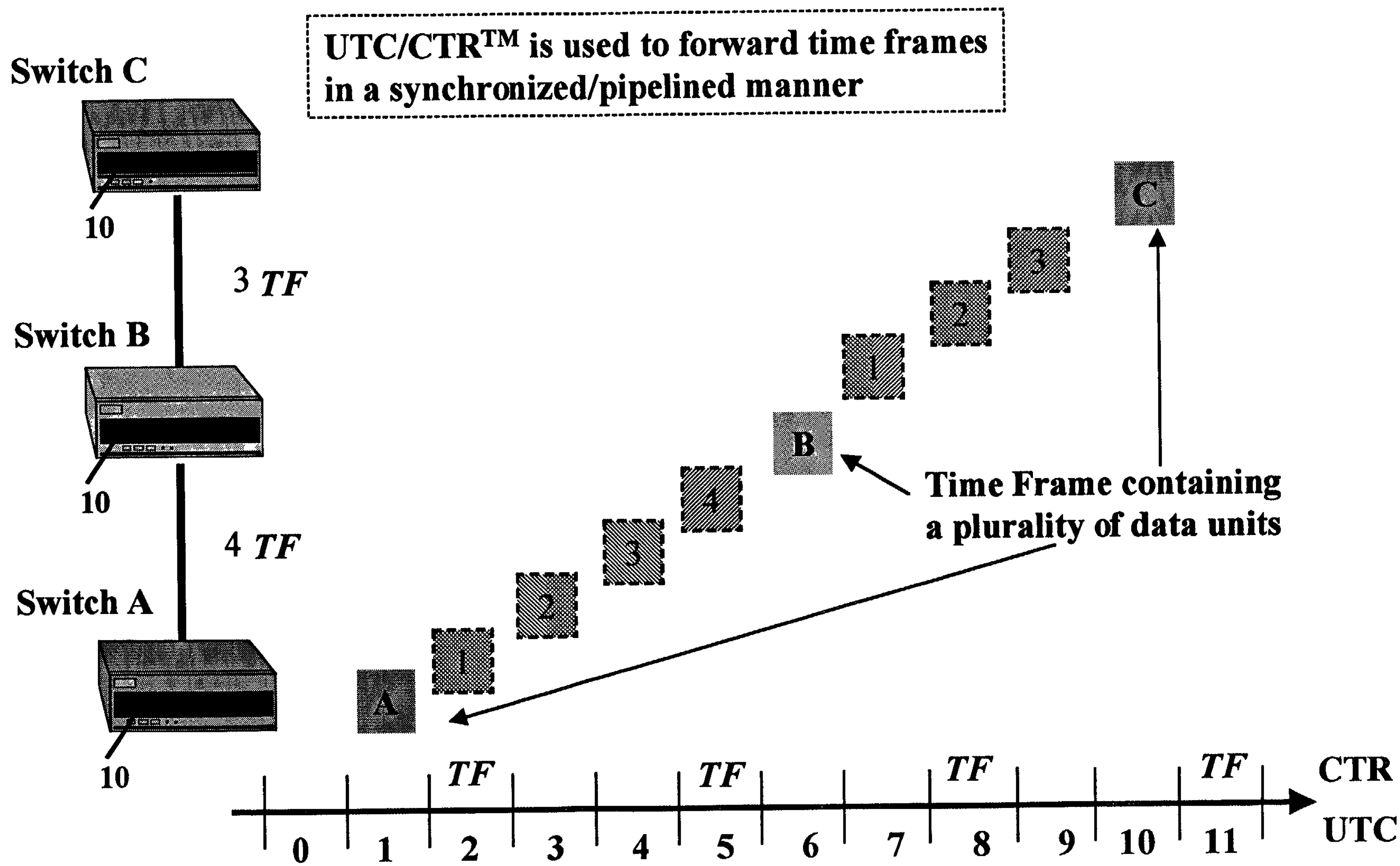
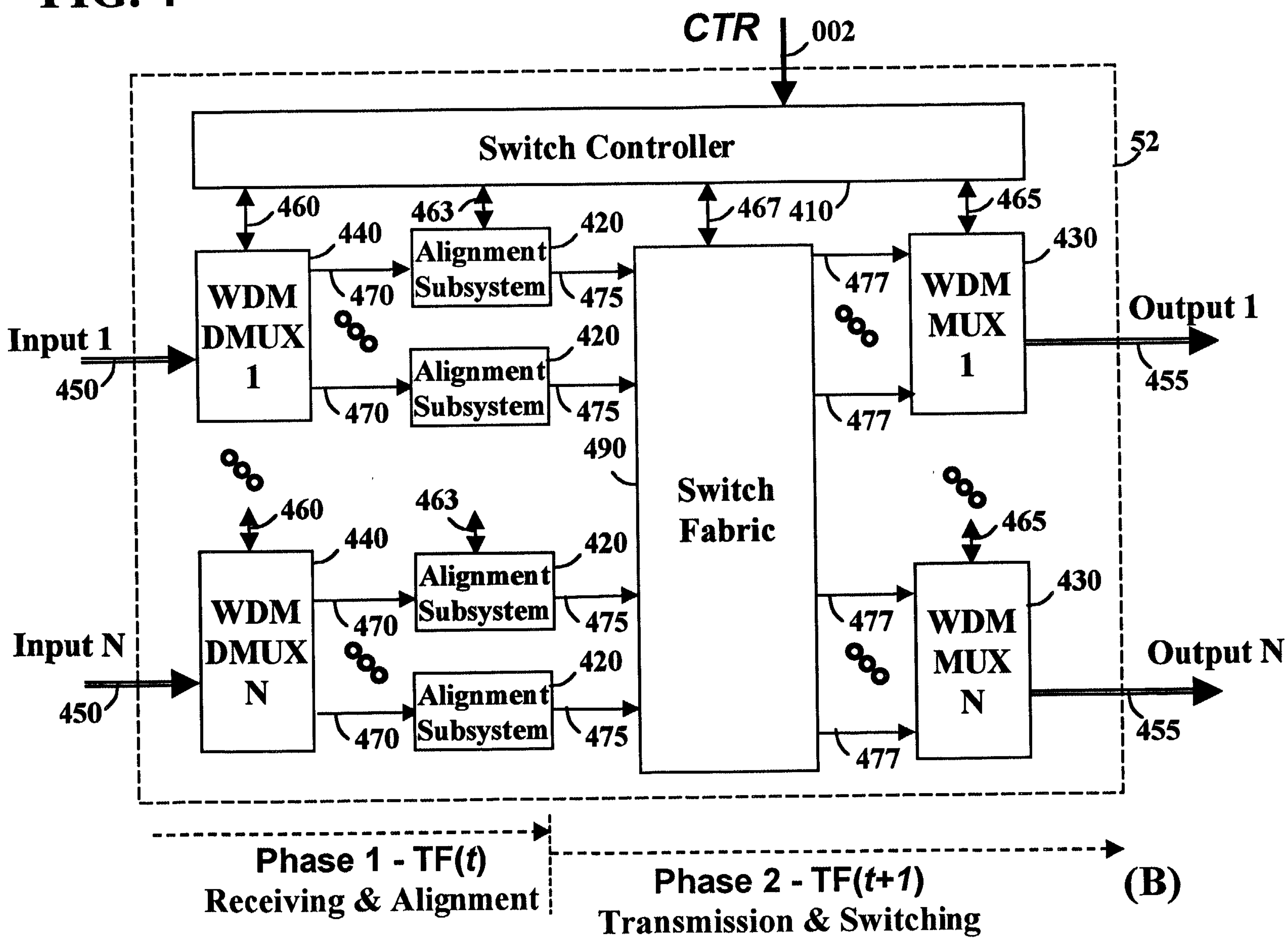

UTC/CTR™ is used to forward time frames in a synchronized/pipelined manner
Switch C
Switch B
Switch A
10
10
10
3 TF
4 TF
A
1
2
3
4
B
1
2
3
C
Time Frame containing a plurality of data units
TF
TF
TF
TF
0
1
2
3
4
5
6
7
8
9
10
11
CTR
UTC

FIG. 4



CTR
002
Switch Controller
52
460
463
467
410
465
440
420
430
WDM DMUX 1
Alignment Subsystem
WDM MUX 1
Input 1
450
470
475
477
Output 1
455
490
Switch Fabric
WDM DMUX N
WDM MUX N
Input N
Output N
Phase 1 - TF(t)
Receiving & Alignment
Phase 2 - TF(t+1)
Transmission & Switching
(B)

FIG. 5

Two time intervals: SC1_length·TF1 = 1 UTC second

- SC2_length·TF2 = 1 UTC second
- TF2 = (SC1_length / SC2_length) · TF1 = k · TF1, where the time cycles of TF1 and TF2 are aligned with respect to UTC.

For ***k*** = 2 and ***c*** = 4 (e.g., High_capacity=OC-192, Low_capacity=OC-48):

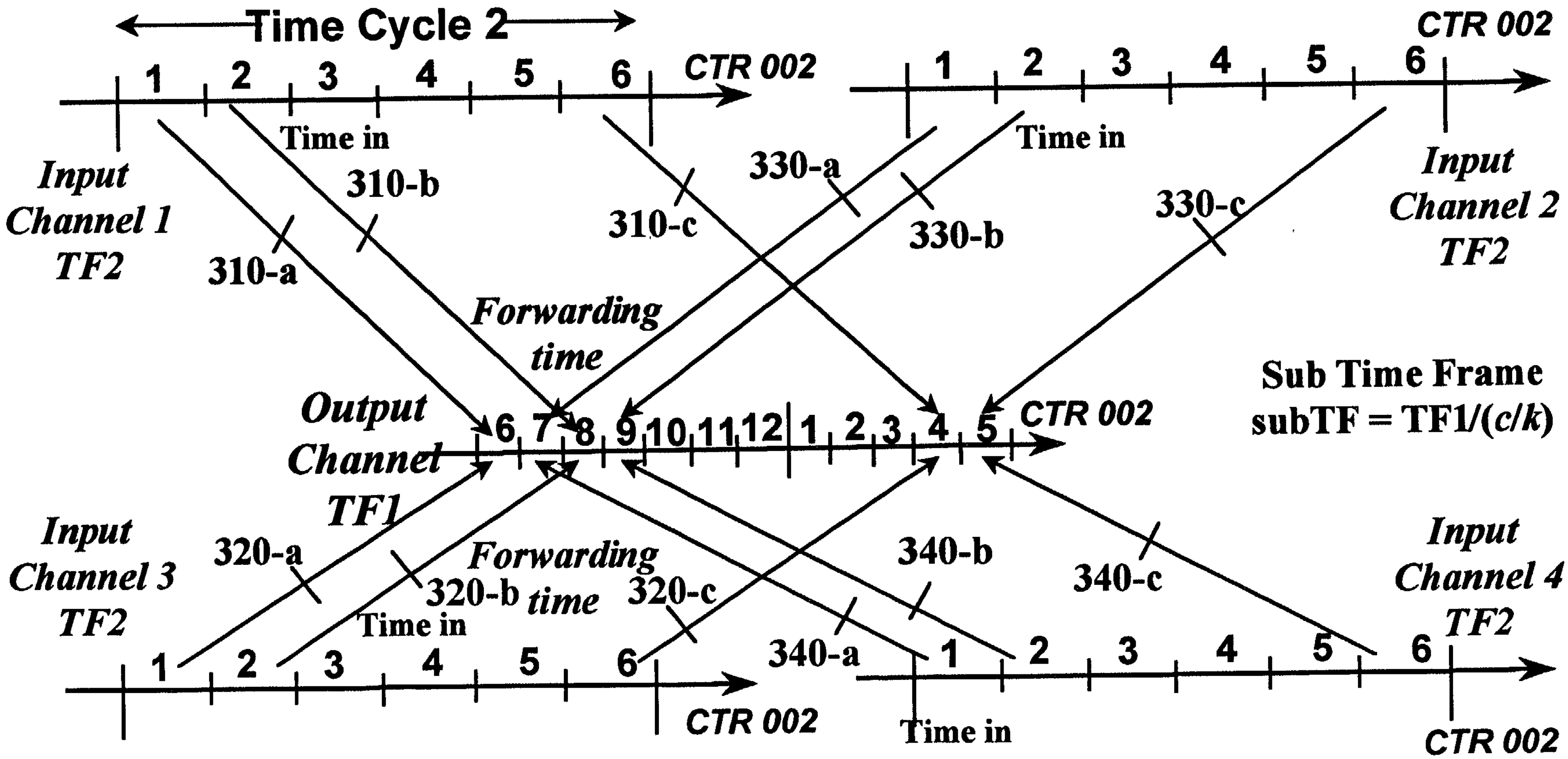


FIG. 6

Two time intervals: $SC1\_length \cdot TF1 = 1$ UTC second

- $SC2\_length \cdot TF2 = 1$ UTC second
- $TF2 = (SC1\_length / SC2\_length) \cdot TF1 = k \cdot TF1$, where the time cycles of $TF1$ and $TF2$ are aligned with respect to UTC.

For $k = 2$ and $c = 4$ (e.g., High_capacity=OC-192, Low_capacity=OC-48):

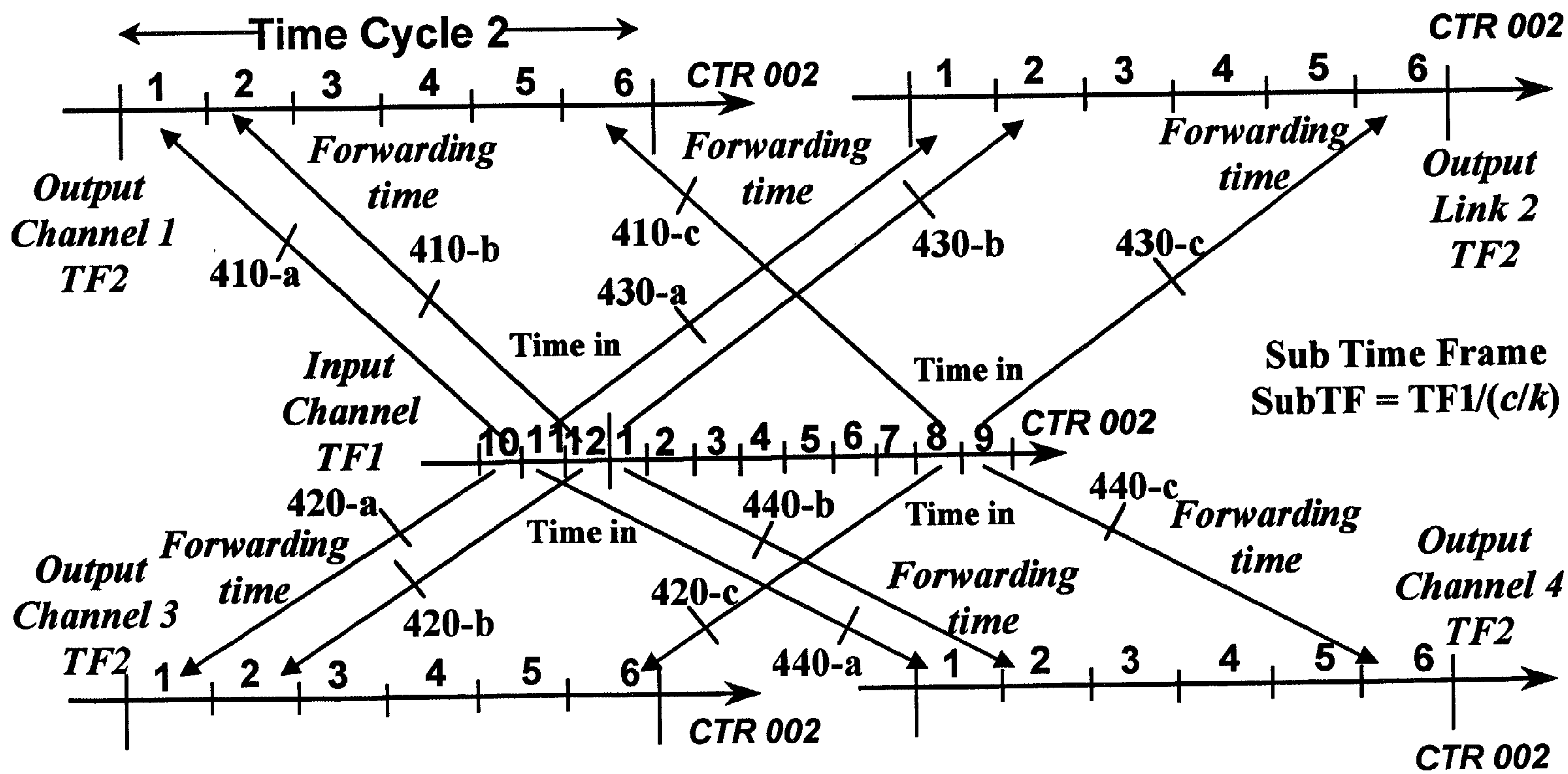


FIG. 7

Two time intervals: $SC1\_length \cdot TF1 = 1$ **UTC second**

- $SC2\_length \cdot TF2 = 1$ **UTC second**
- $TF2 = (SC1\_length / SC2\_length) \cdot TF1 = k \cdot TF1$, **where the time cycles of** $TF1$ **and** $TF2$ **are aligned with respect to UTC.**

For $k = 2$ **and** $c = 4$ **(e.g., High_capacity=OC-192, Low_capacity=OC-48):**

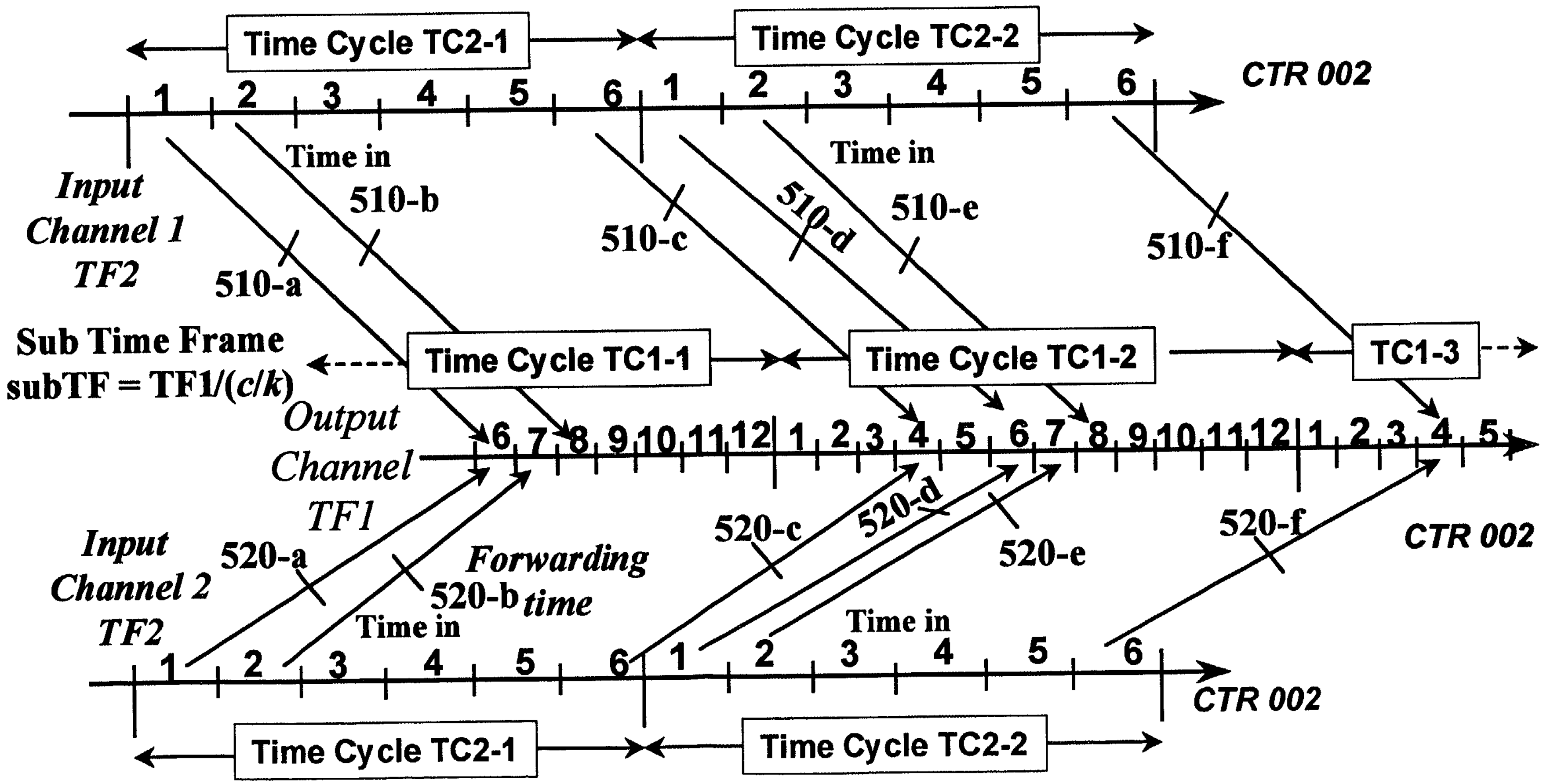


FIG. 8

Two time intervals: $SC1\_length \cdot TF1 = 1$ UTC second

- $SC2\_length \cdot TF2 = 1$ UTC second
- $TF2 = (SC1\_length / SC2\_length) \cdot TF1 = k \cdot TF1$, where the time cycles of $TF1$ and $TF2$ are aligned with respect to UTC.

For $k = 2$ and $c = 4$ (e.g., High_capacity=OC-192, Low_capacity=OC-48):

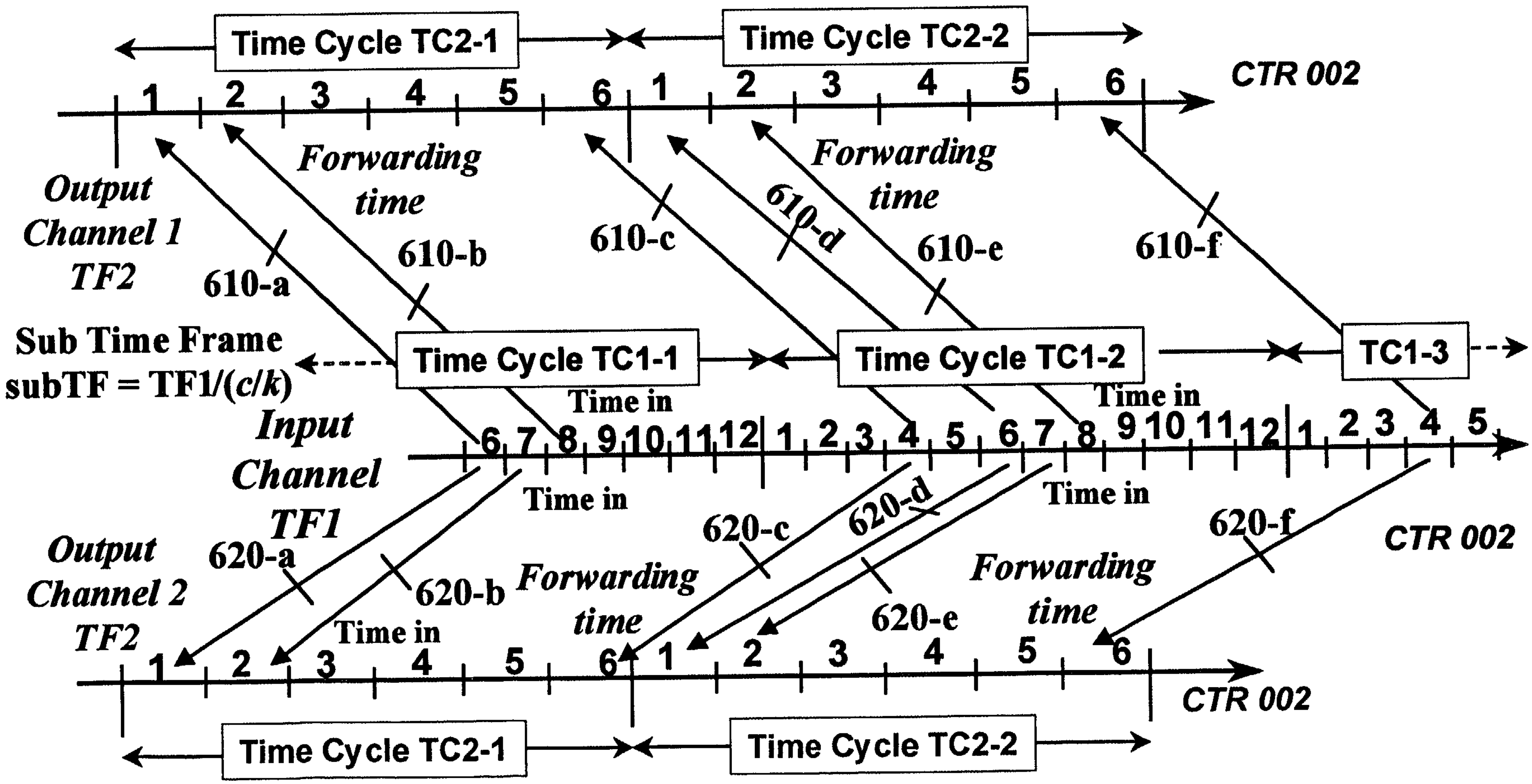


FIG. 9

c=4, e.g., OC-192/OC-48
k=2, e.g., 25 microsec/12.5 microsec

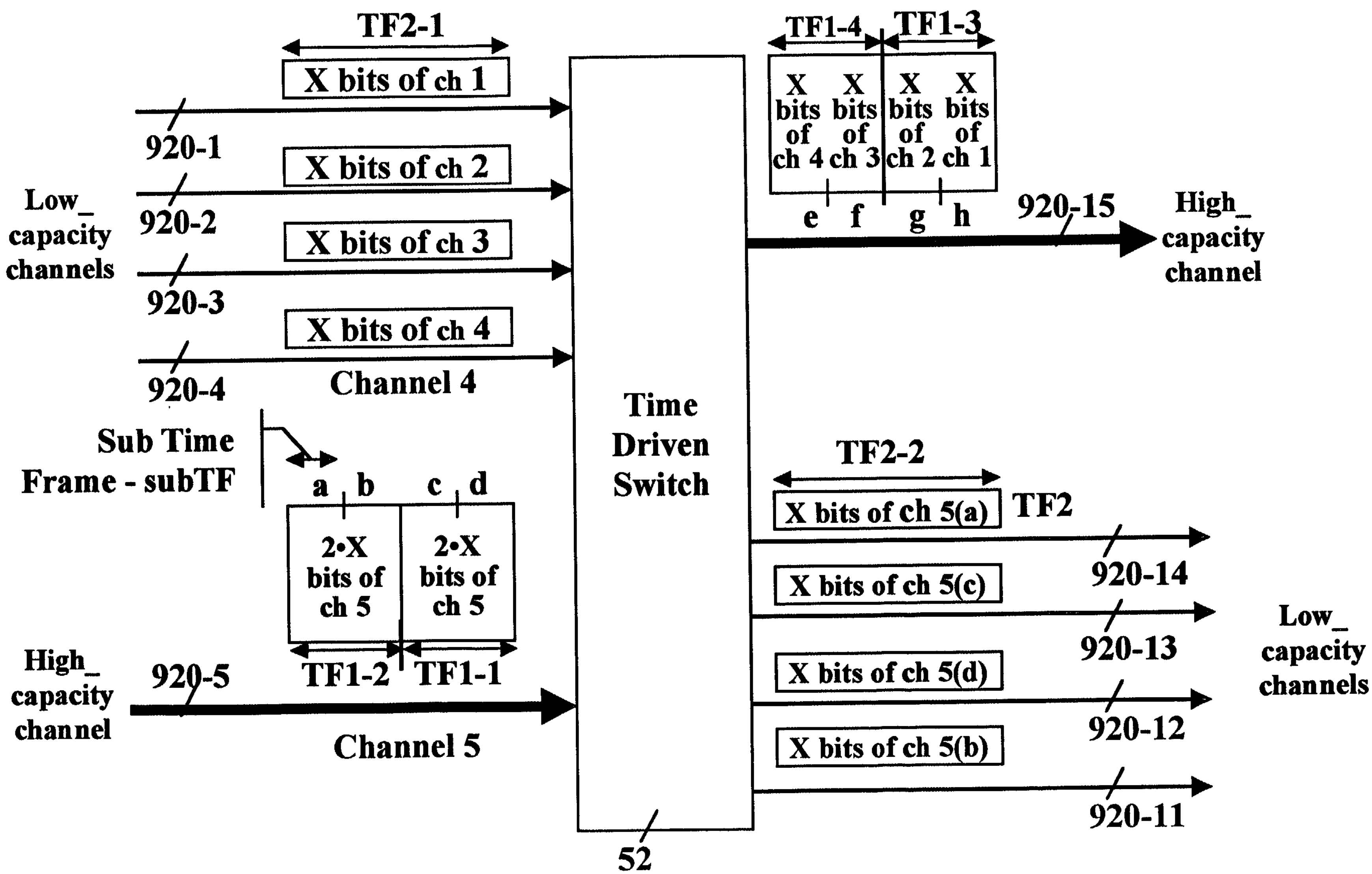


FIG. 10

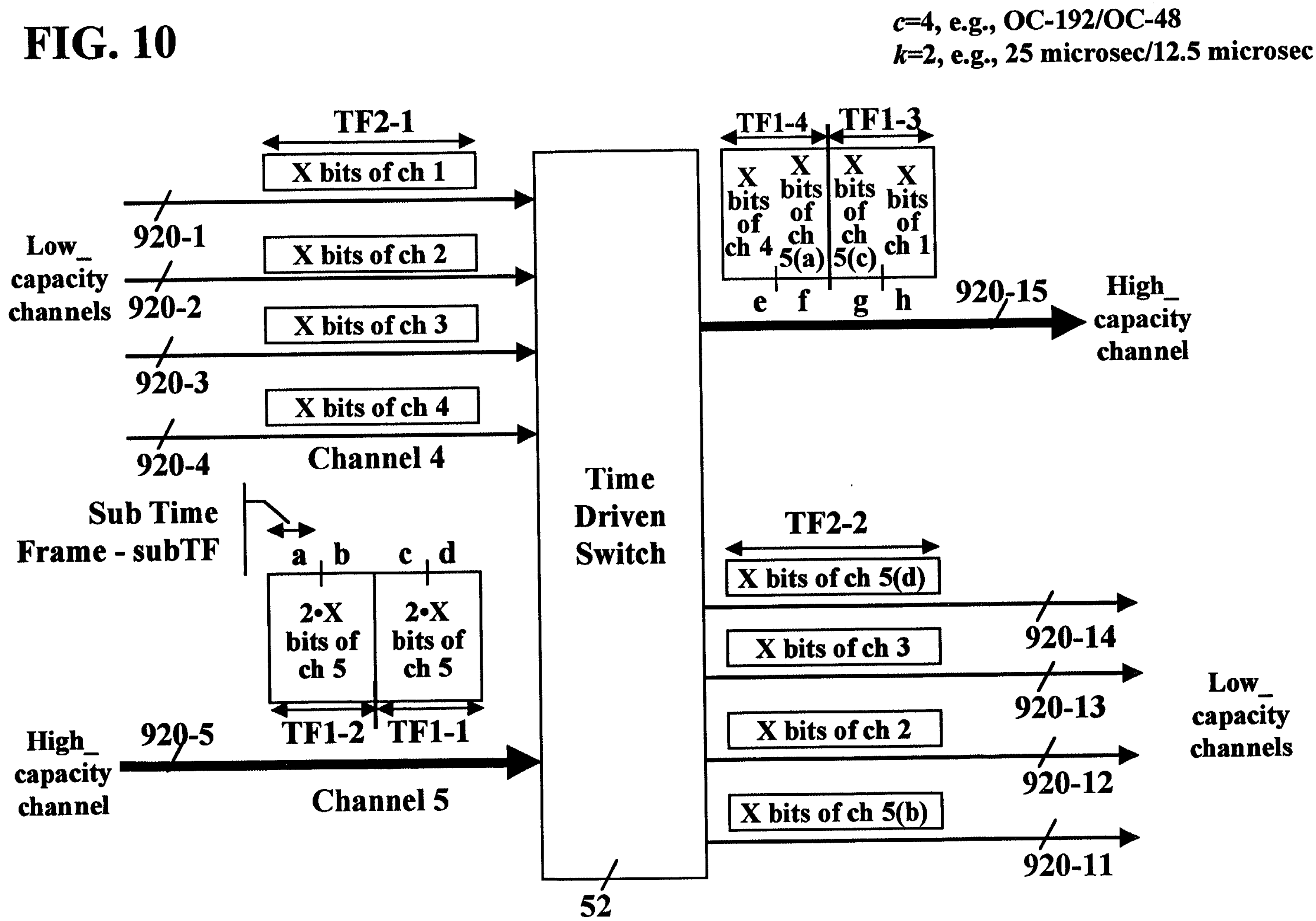

c=4, e.g., OC-192/OC-48
k=2, e.g., 25 microsec/12.5 microsec
TF2-1
X bits of ch 1
X bits of ch 2
X bits of ch 3
X bits of ch 4
Channel 4
Low_ capacity channels
920-1
920-2
920-3
920-4
Sub Time Frame - subTF
a
b
c
d
2•X bits of ch 5
2•X bits of ch 5
TF1-2
TF1-1
High_ capacity channel
920-5
Channel 5
Time Driven Switch
52
TF1-4
TF1-3
X bits of ch 4
X bits of ch 5(a)
X bits of ch 5(c)
X bits of ch 1
e
f
g
h
920-15
High_ capacity channel
TF2-2
X bits of ch 5(d)
X bits of ch 3
X bits of ch 2
X bits of ch 5(b)
920-14
920-13
920-12
920-11
Low_ capacity channels

FIG. 11

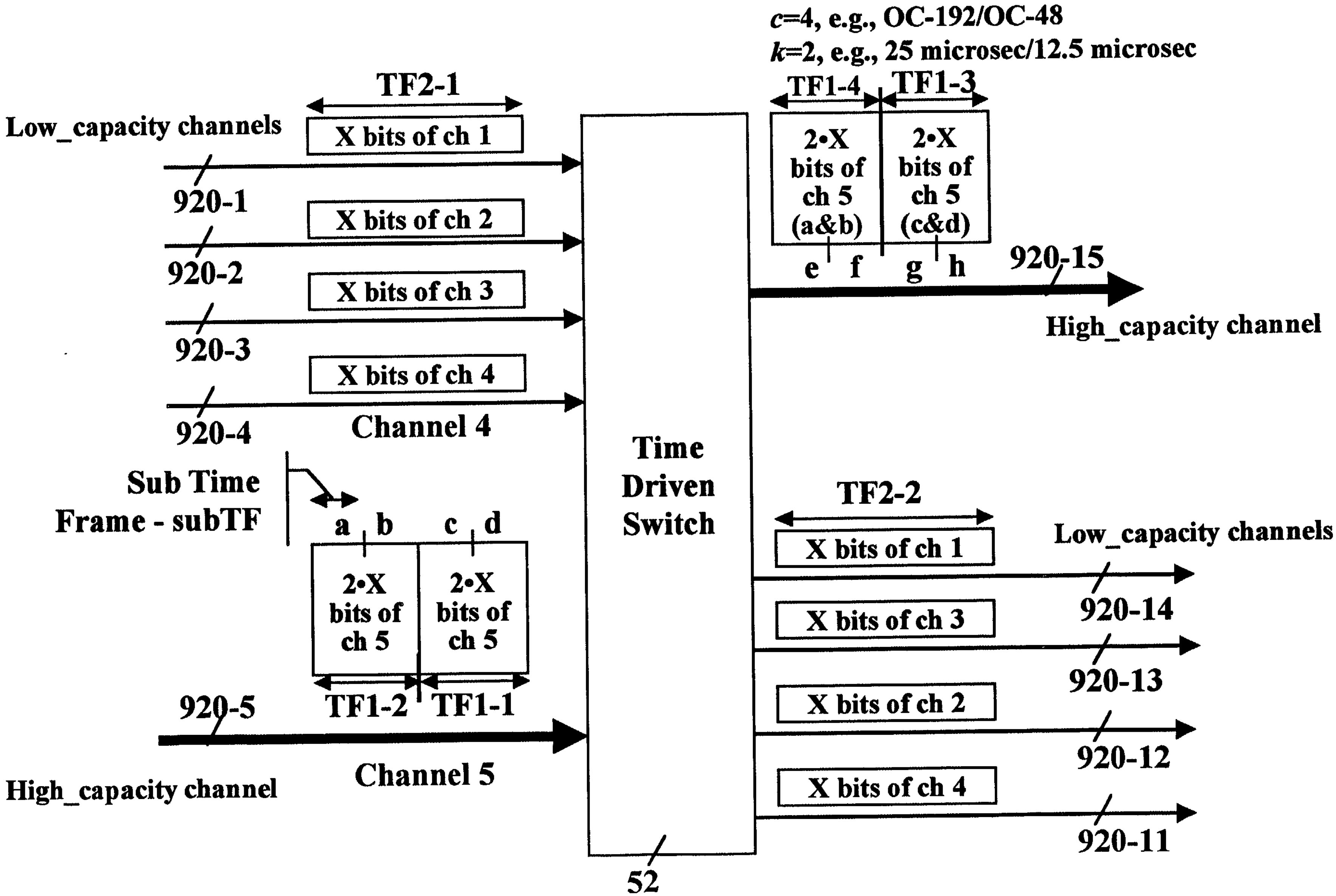

c=4, e.g., OC-192/OC-48
k=2, e.g., 25 microsec/12.5 microsec
TF2-1
Low_capacity channels
X bits of ch 1
920-1
X bits of ch 2
920-2
X bits of ch 3
920-3
X bits of ch 4
920-4
Channel 4
Sub Time
Frame - subTF
a b c d
2•X bits of ch 5
2•X bits of ch 5
TF1-2
TF1-1
920-5
High_capacity channel
Channel 5
Time
Driven
Switch
52
TF1-4
TF1-3
2•X bits of ch 5 (a&b)
2•X bits of ch 5 (c&d)
e f g h
920-15
High_capacity channel
TF2-2
Low_capacity channels
X bits of ch 1
920-14
X bits of ch 3
920-13
X bits of ch 2
920-12
X bits of ch 4
920-11

FIG. 12

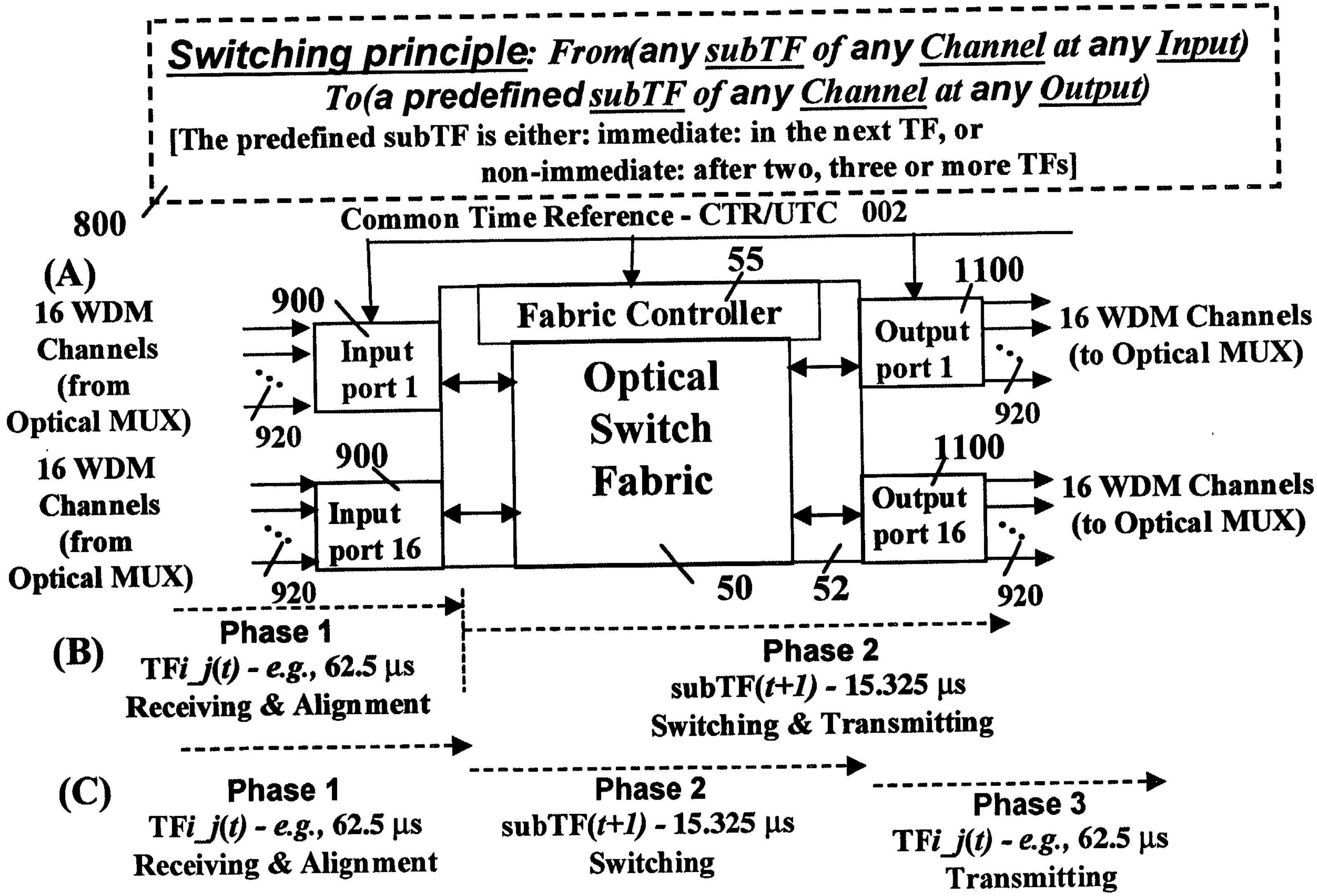
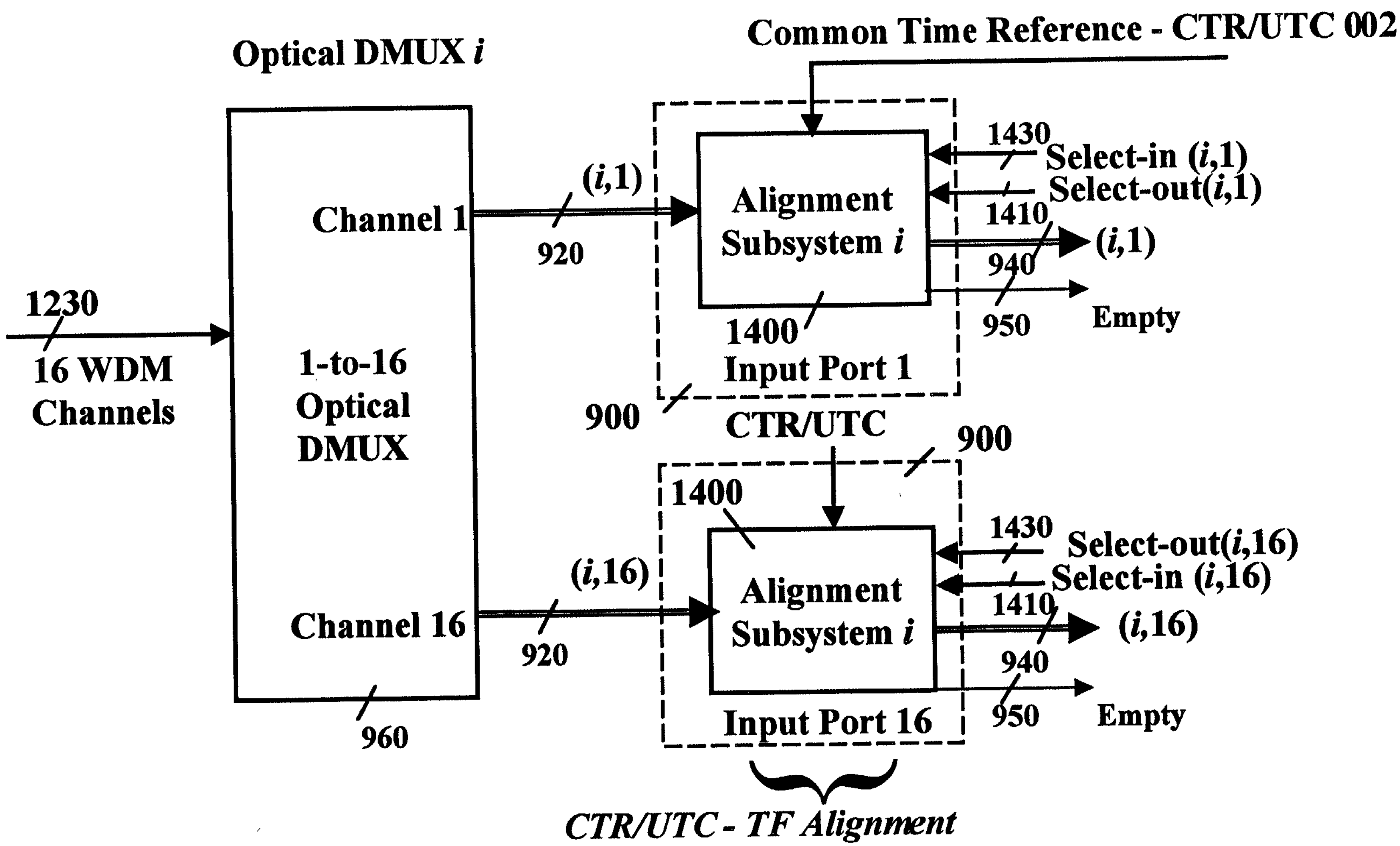

Switching principle: From(any subTF of any Channel at any Input)
To(a predefined subTF of any Channel at any Output)
[The predefined subTF is either: immediate: in the next TF, or
non-immediate: after two, three or more TFs]
800
Common Time Reference - CTR/UTC 002
(A)
16 WDM Channels (from Optical MUX)
900
920
Input port 1
16 WDM Channels (from Optical MUX)
900
920
Input port 16
55
Fabric Controller
Optical Switch Fabric
50
52
1100
Output port 1
920
16 WDM Channels (to Optical MUX)
1100
Output port 16
920
16 WDM Channels (to Optical MUX)
(B)
Phase 1
TFi_j(t) - e.g., 62.5 μs
Receiving & Alignment
Phase 2
subTF(t+1) - 15.325 μs
Switching & Transmitting
(C)
Phase 1
TFi_j(t) - e.g., 62.5 μs
Receiving & Alignment
Phase 2
subTF(t+1) - 15.325 μs
Switching
Phase 3
TFi_j(t) - e.g., 62.5 μs
Transmitting

FIG. 13



Optical DMUX *i*
1230
16 WDM Channels
1-to-16 Optical DMUX
Channel 1
Channel 16
960
(*i*,1)
920
(*i*,16)
920
Common Time Reference - CTR/UTC 002
Alignment Subsystem *i*
1400
Input Port 1
900
CTR/UTC
900
1400
Alignment Subsystem *i*
Input Port 16
1430
Select-in (*i*,1)
Select-out(*i*,1)
1410
(*i*,1)
940
950
Empty
1430
Select-out(*i*,16)
Select-in (*i*,16)
1410
(*i*,16)
940
950
Empty
CTR/UTC - TF Alignment

FIG. 14

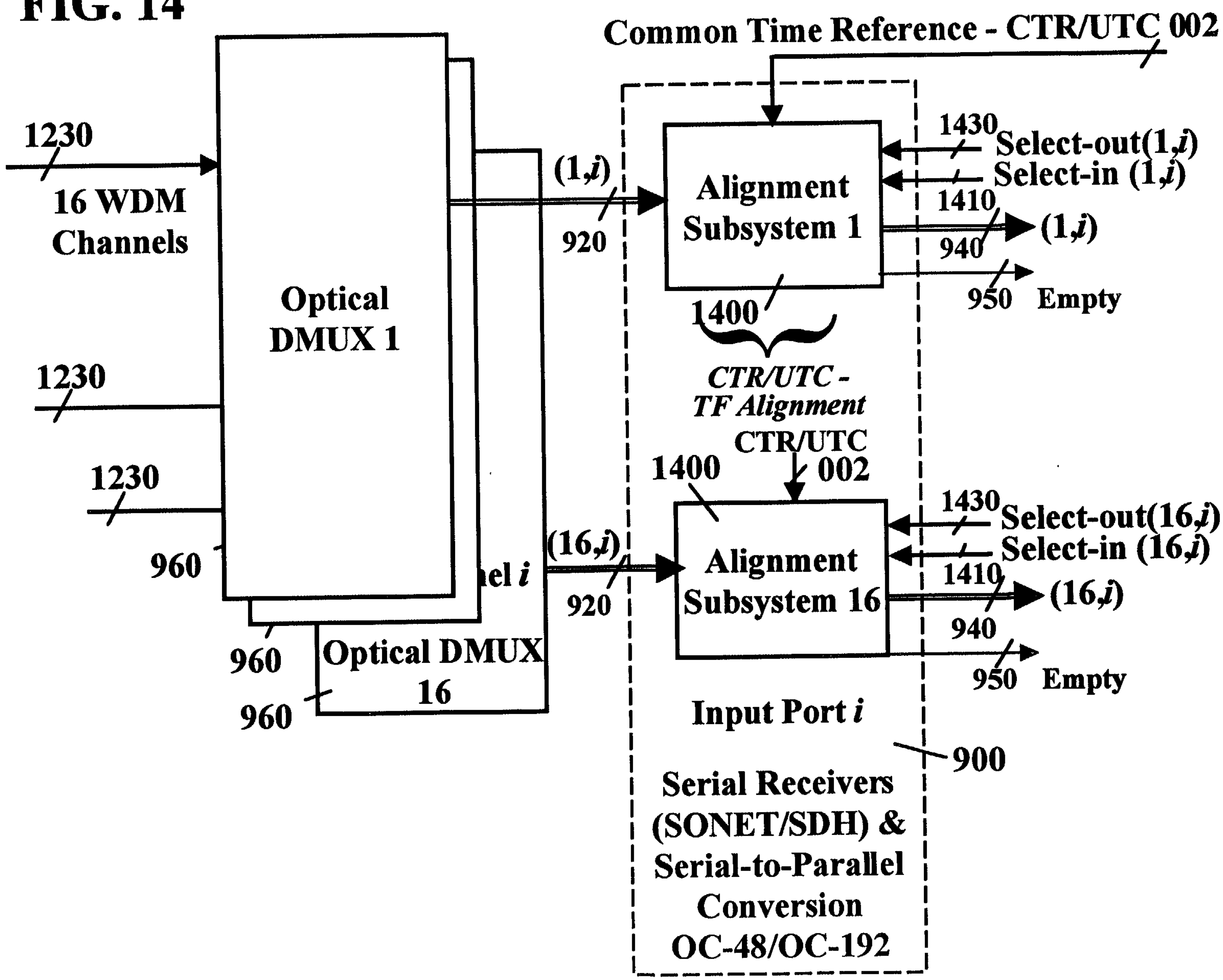

Common Time Reference - CTR/UTC 002
1230
16 WDM Channels
1230
1230
960
960
960
Optical DMUX 1
Optical DMUX 16
nel i
(1,i)
920
(16,i)
920
Alignment Subsystem 1
Alignment Subsystem 16
1400
1400
CTR/UTC - TF Alignment
CTR/UTC 002
1430
Select-out(1,i)
Select-in (1,i)
1410
940
(1,i)
950
Empty
1430
Select-out(16,i)
Select-in (16,i)
1410
940
(16,i)
950
Empty
Input Port i
900
Serial Receivers (SONET/SDH) & Serial-to-Parallel Conversion OC-48/OC-192

FIG. 15

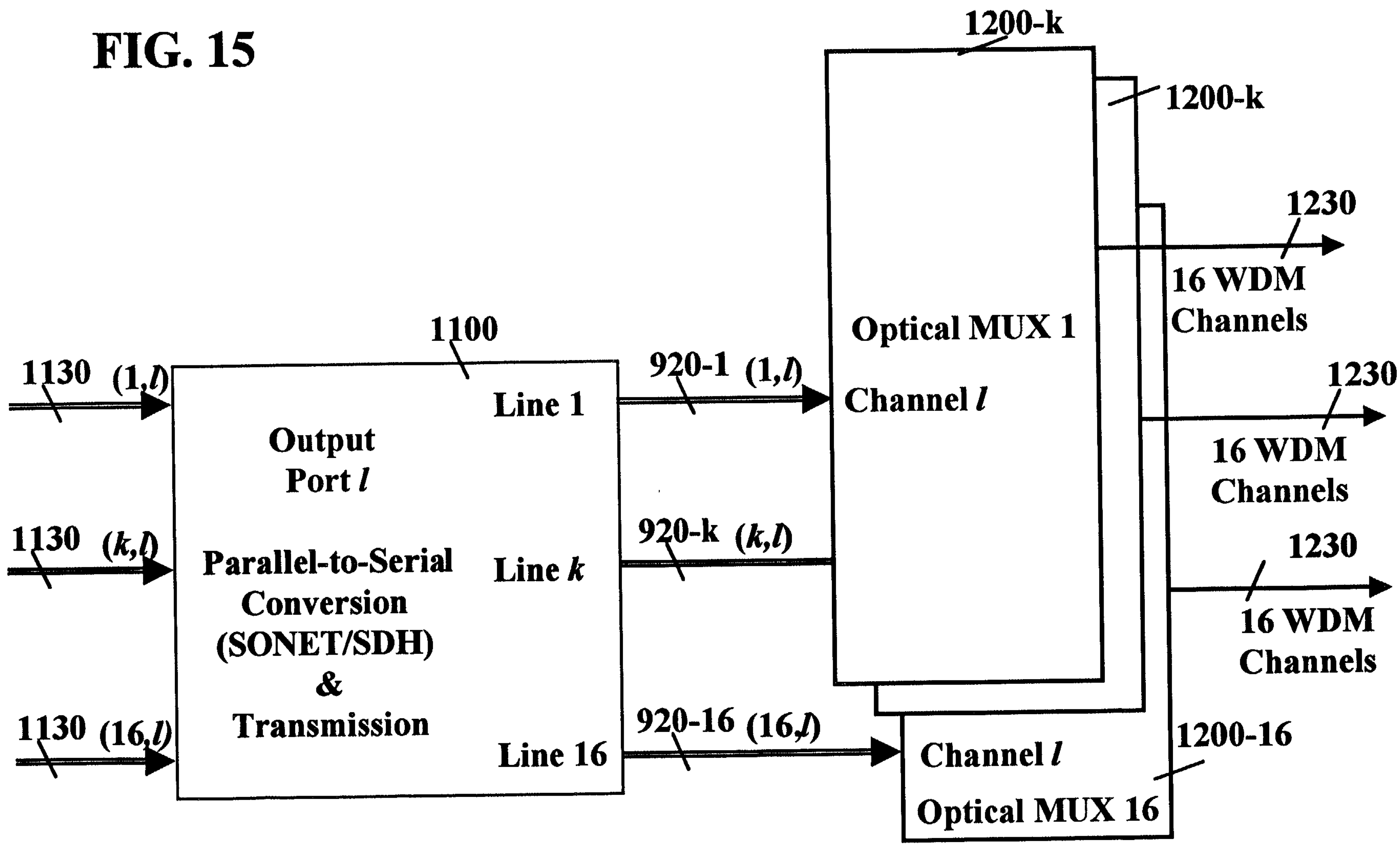

1130 (1,l)
1130 (k,l)
1130 (16,l)
1100
Output
Port l
Parallel-to-Serial
Conversion
(SONET/SDH)
&
Transmission
Line 1
Line k
Line 16
920-1 (1,l)
920-k (k,l)
920-16 (16,l)
1200-k
1200-k
Optical MUX 1
Channel l
Channel l
Optical MUX 16
1200-16
1230
16 WDM
Channels
1230
16 WDM
Channels
1230
16 WDM
Channels

FIG. 16

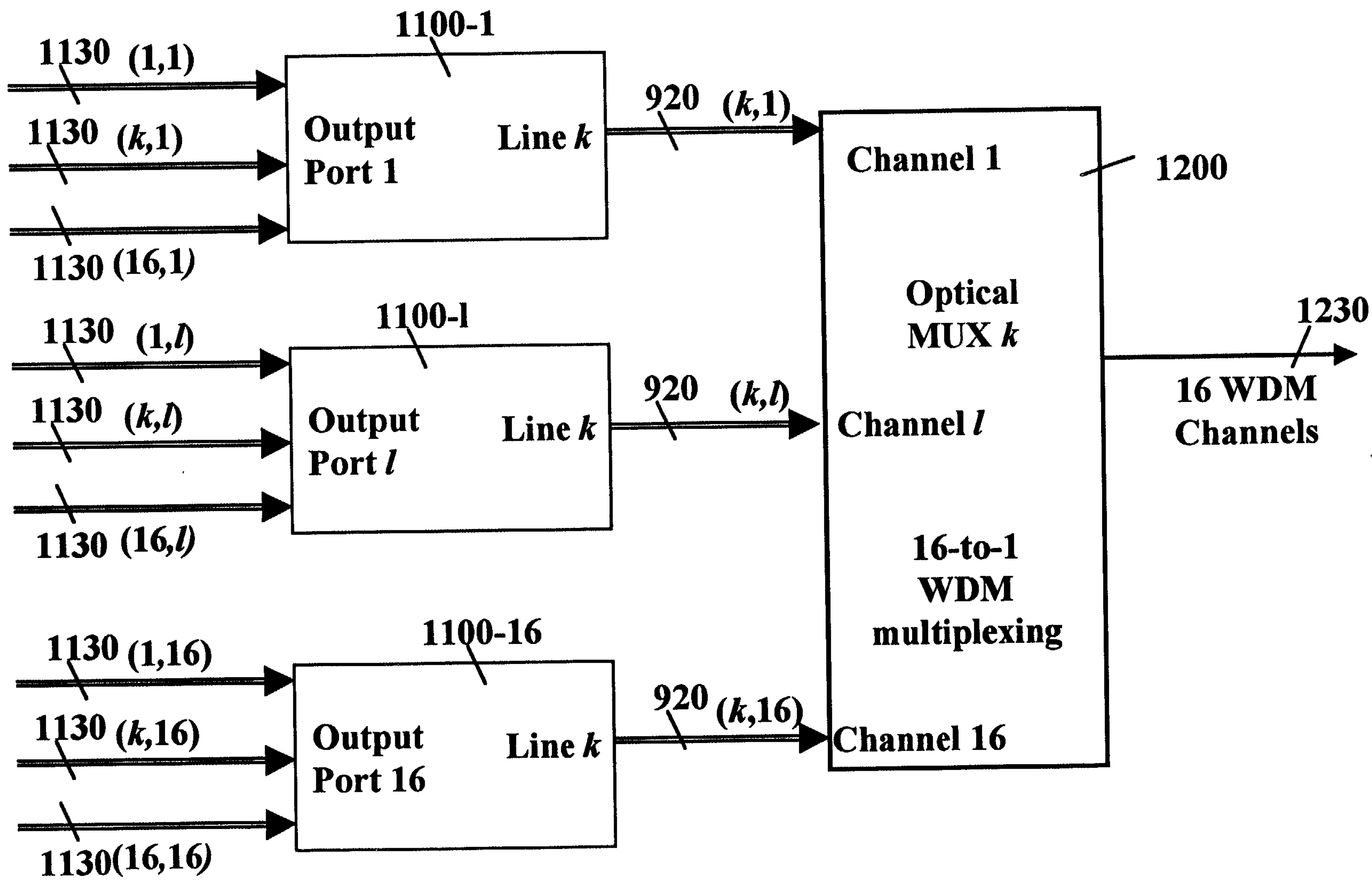

1100-1
1130 (1,1)
1130 (k,1)
1130 (16,1)
Output Port 1
Line k
920 (k,1)
1100-l
1130 (1,l)
1130 (k,l)
1130 (16,l)
Output Port l
Line k
920 (k,l)
1100-16
1130 (1,16)
1130 (k,16)
1130(16,16)
Output Port 16
Line k
920 (k,16)
Channel 1
1200
Optical MUX k
Channel l
16-to-1 WDM multiplexing
Channel 16
1230
16 WDM Channels

FIG. 17

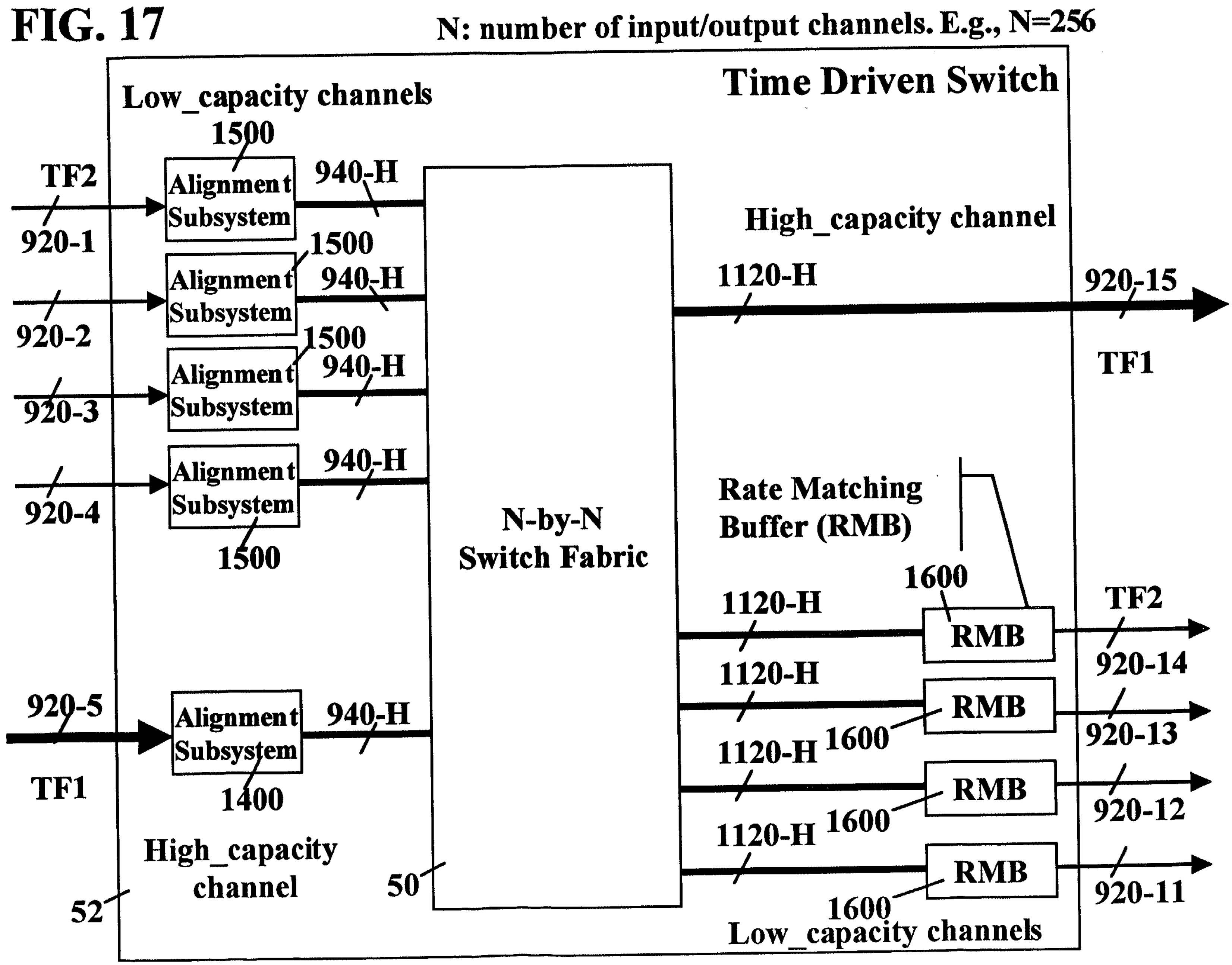
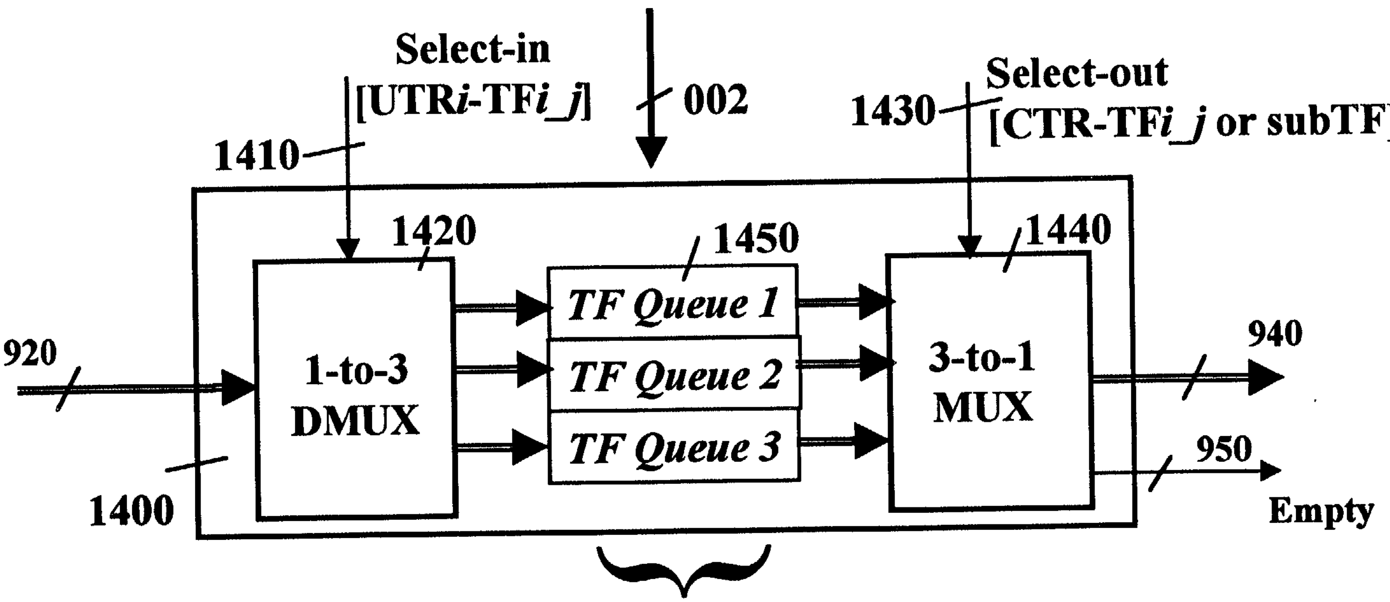

N: number of input/output channels. E.g., N=256
Time Driven Switch
Low_capacity channels
1500
TF2
920-1
Alignment Subsystem
940-H
1500
920-2
Alignment Subsystem
940-H
1500
920-3
Alignment Subsystem
940-H
920-4
Alignment Subsystem
940-H
1500
920-5
TF1
Alignment Subsystem
940-H
1400
High_capacity channel
52
50
N-by-N Switch Fabric
High_capacity channel
1120-H
920-15
TF1
Rate Matching Buffer (RMB)
1600
1120-H
RMB
TF2
920-14
1120-H
RMB
1600
920-13
1120-H
RMB
1600
920-12
1120-H
RMB
1600
920-11
Low_capacity channels

FIG. 18

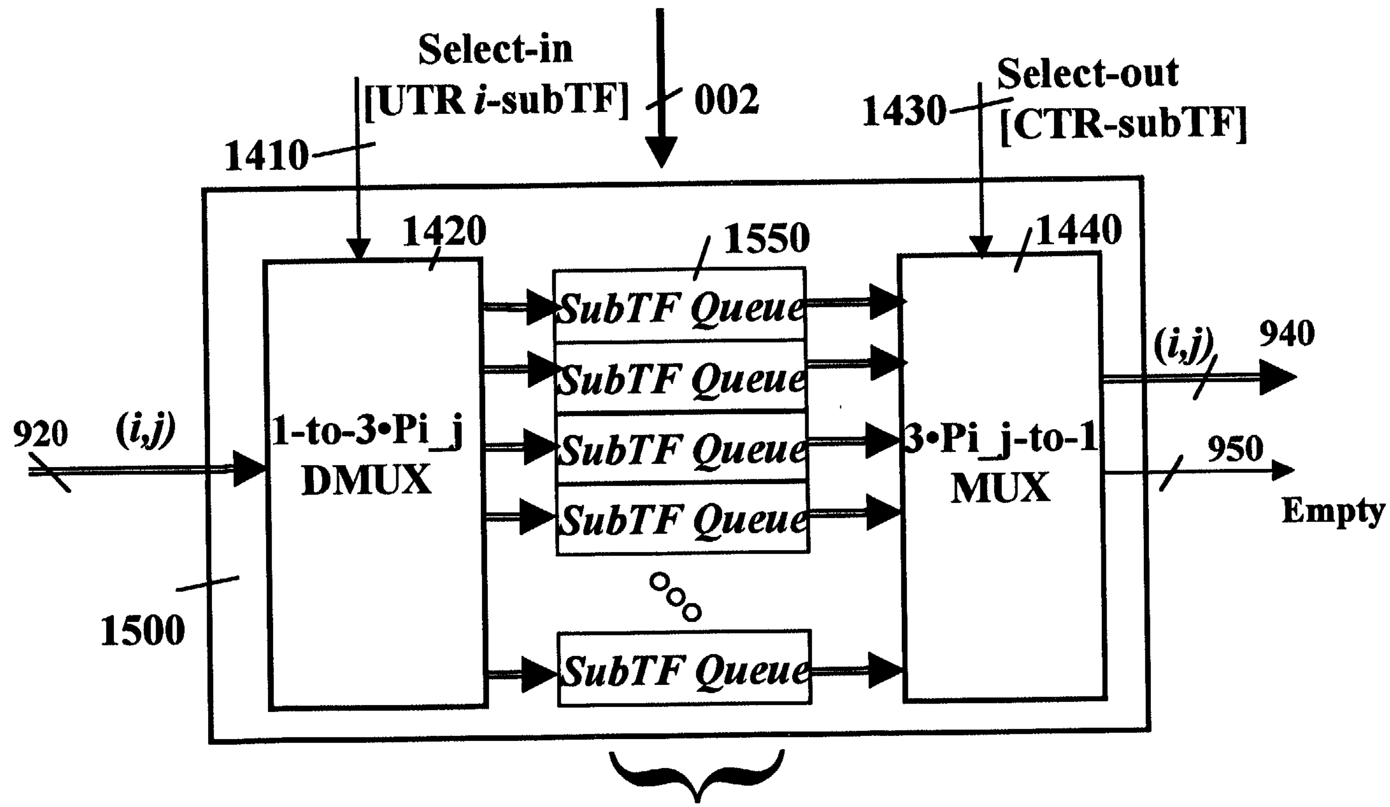
TFi_j: Time frame duration on channel j at Input Interface i.
UTRi: UTR on link connected to Input Interface i
Common Time Reference - CTR/UTC



Alignment Subsystem for Channel j at Input Interface i
with a Plurality of __Time Frame Queues__

FIG. 19

TFi_j: Time frame duration on channel j at Input Interface i.
UTR i: UTR on link connected to Input Interface i
Pi_j = TFi_j/subTF



Alignment Subsystem for *high capacity* Channel *j* at Input Interface *i*
with a Plurality of <u>Sub-Time Frame Queues</u>

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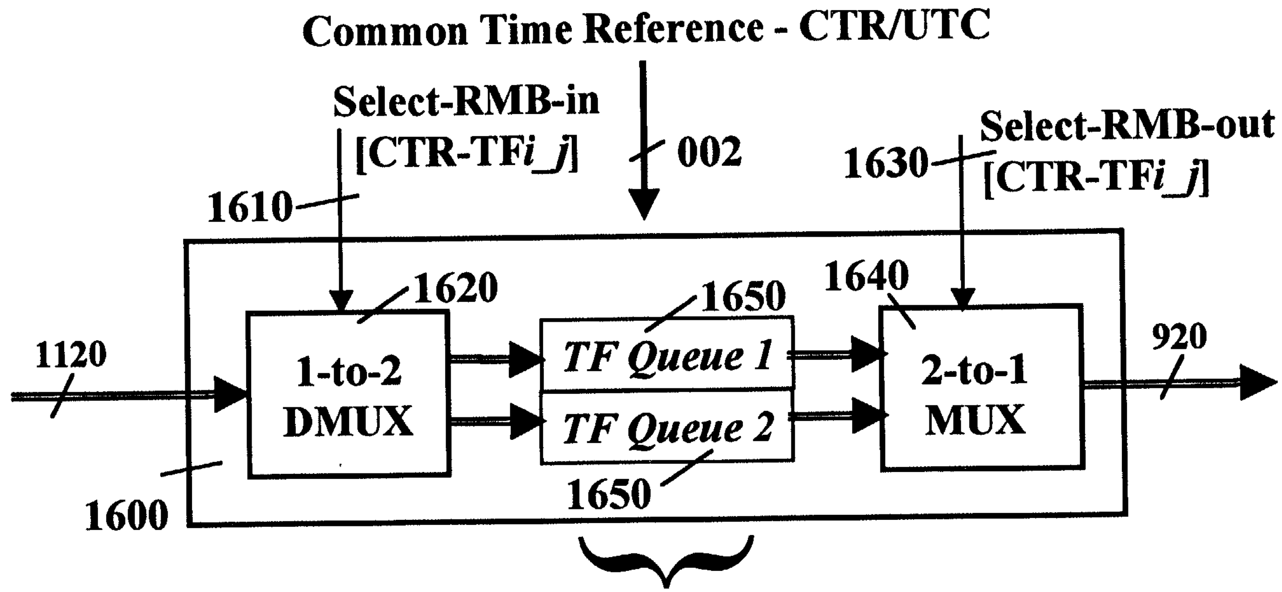
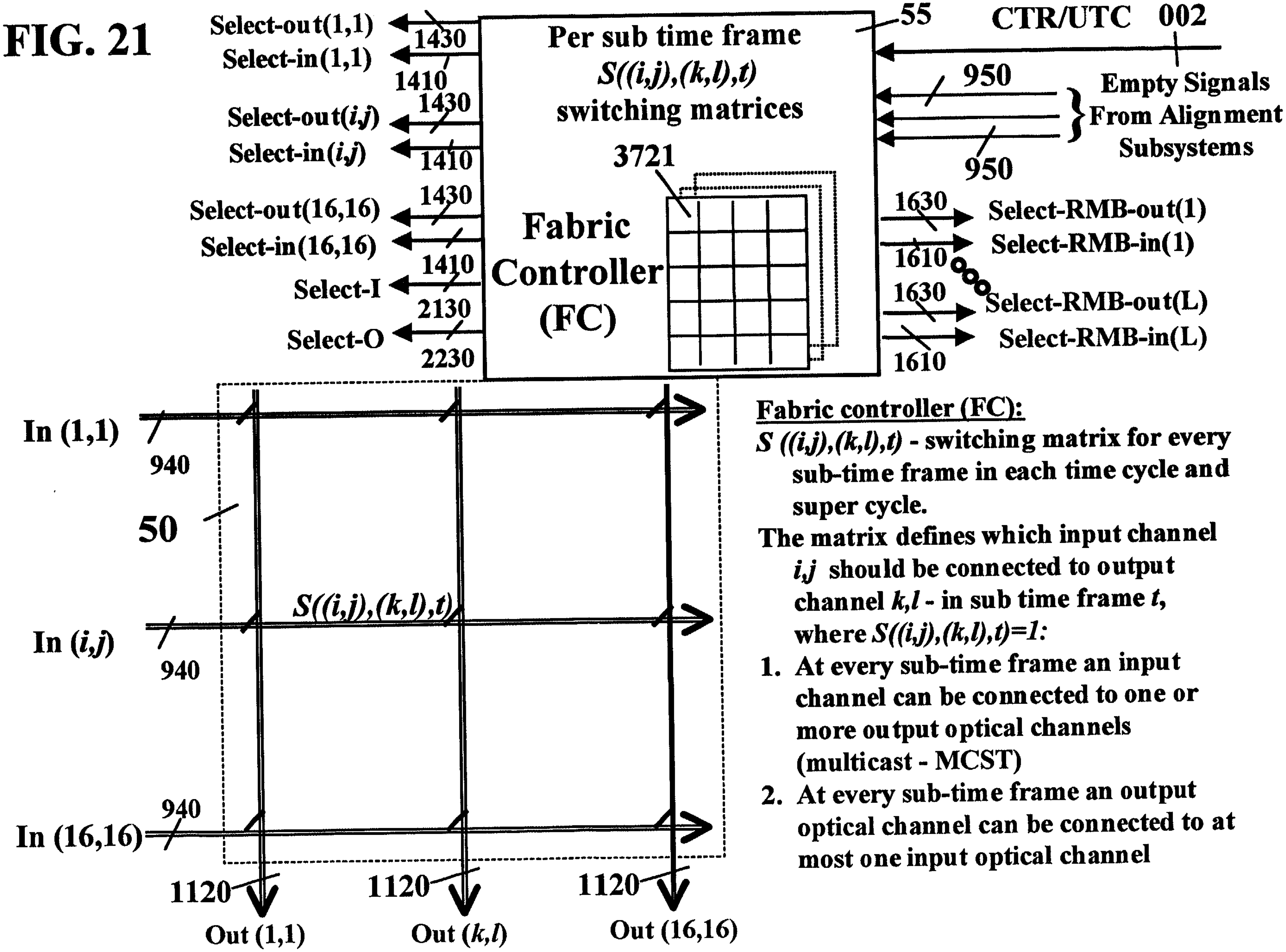
FIG. 18+2 TFi_j: Time frame duration on channel j at Input Interface i.
UTRi: UTR on link connected to Input Interface i



Rate Matching Buffer for Channel j at Output Interface i
with a Plurality of <u>Time Frame Queues</u>
(Also single buffer with dual access memory with single phase switching and forwarding)

FIG. 21



<u>**Fabric controller (FC):**</u>

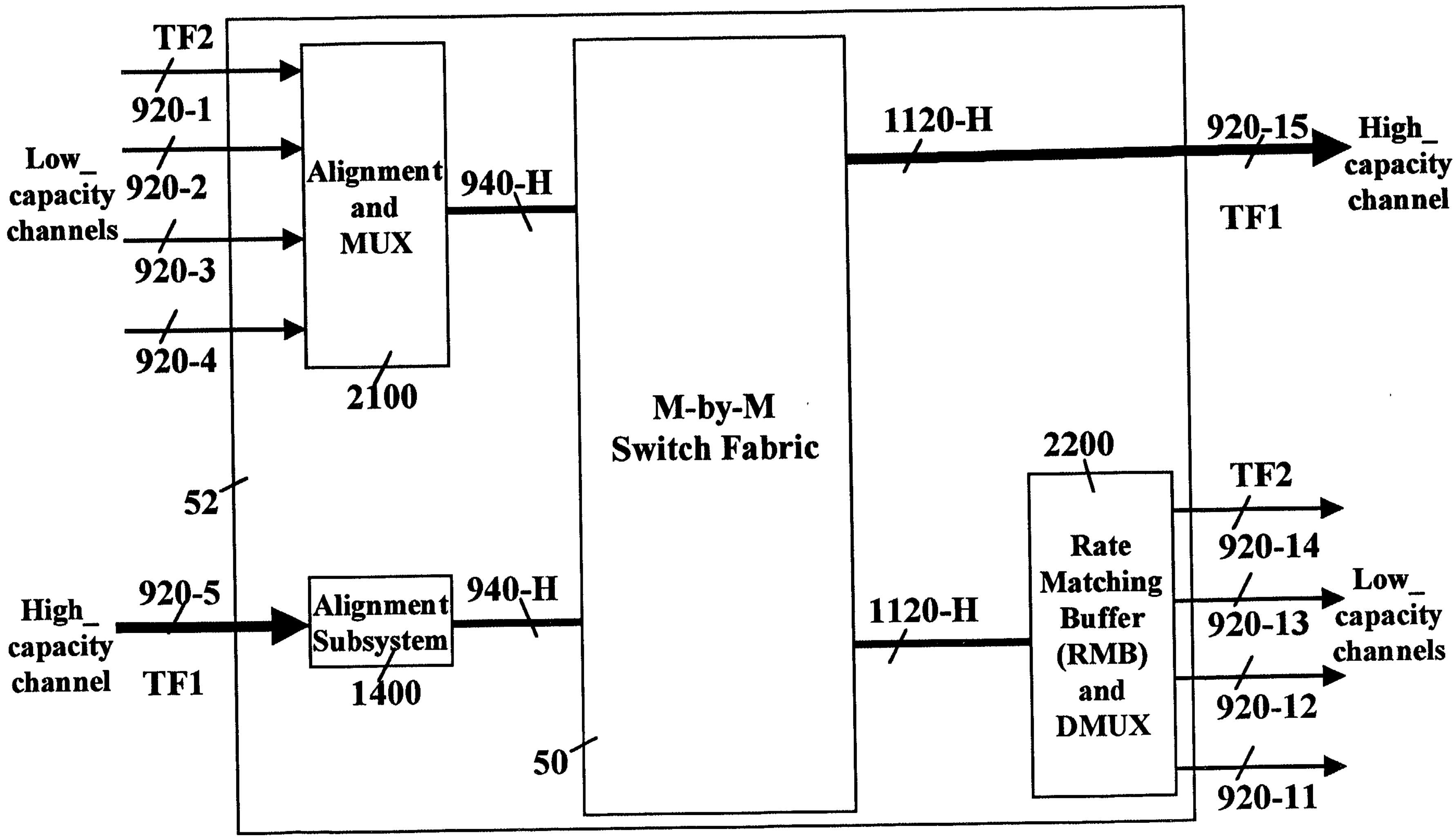
S ((i,j),(k,l),t) **- switching matrix for every sub-time frame in each time cycle and super cycle.**

The matrix defines which input channel *i,j* should be connected to output channel *k,l* - in sub time frame *t*, where *S((i,j),(k,l),t)=1*:

1. **At every sub-time frame an input channel can be connected to one or more output optical channels (multicast - MCST)**
2. **At every sub-time frame an output optical channel can be connected to at most one input optical channel**

FIG. 22

N: number of input/output channels. E.g., N=256
M • High_capacity = N_high • High_capacity + N_low • Low_capacity
M<N



Time Driven Switch

FIG. 23

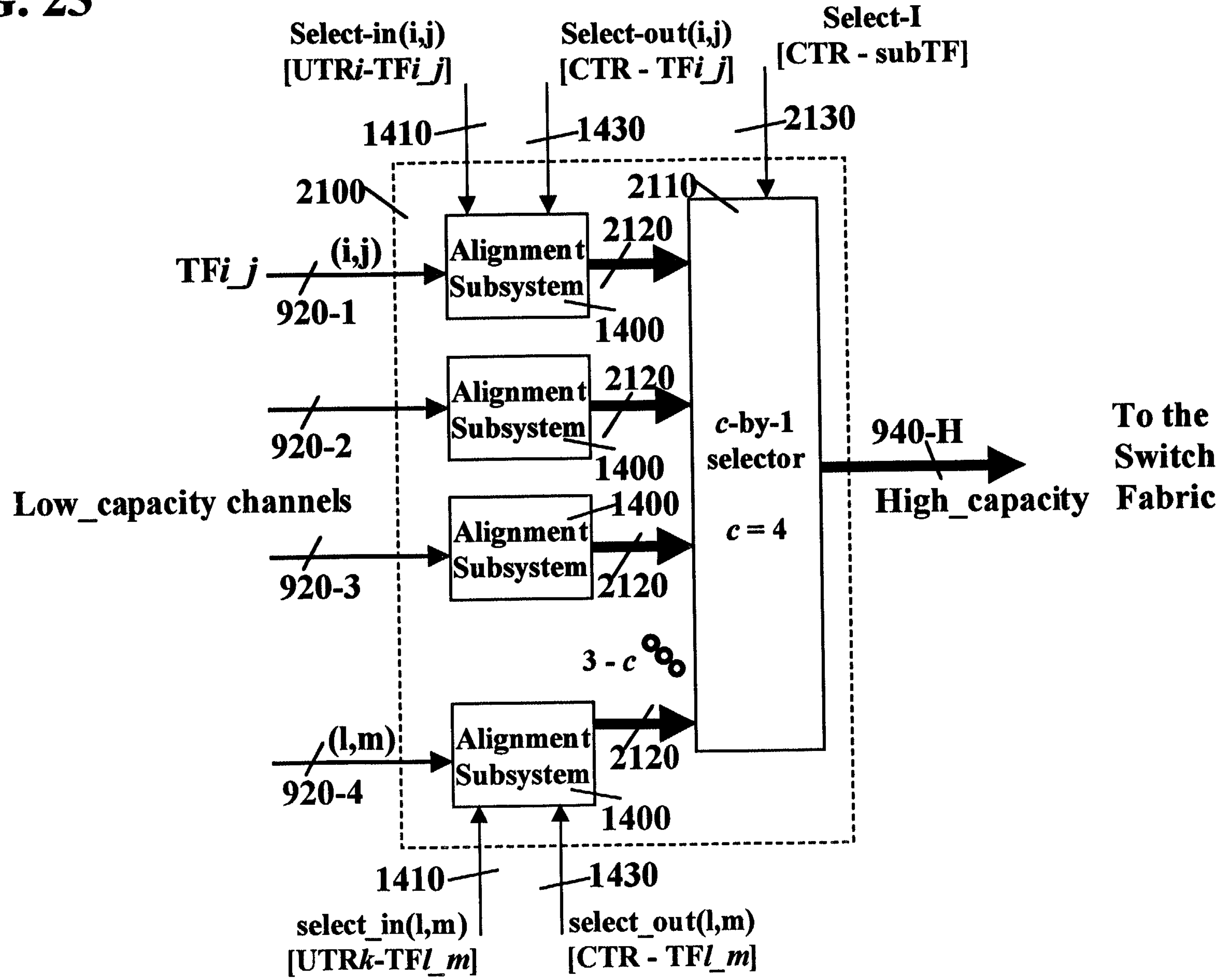

Select-in(i,j)
[UTRi-TFi_j]
Select-out(i,j)
[CTR - TFi_j]
Select-I
[CTR - subTF]
1410
1430
2130
2100
2110
TFi_j
(i,j)
920-1
Alignment Subsystem
2120
1400
920-2
920-3
Low_capacity channels
c-by-1 selector
c = 4
940-H
High_capacity
To the Switch Fabric
3 - c
(l,m)
920-4
select_in(l,m)
[UTRk-TFl_m]
select_out(l,m)
[CTR - TFl_m]

FIG. 24

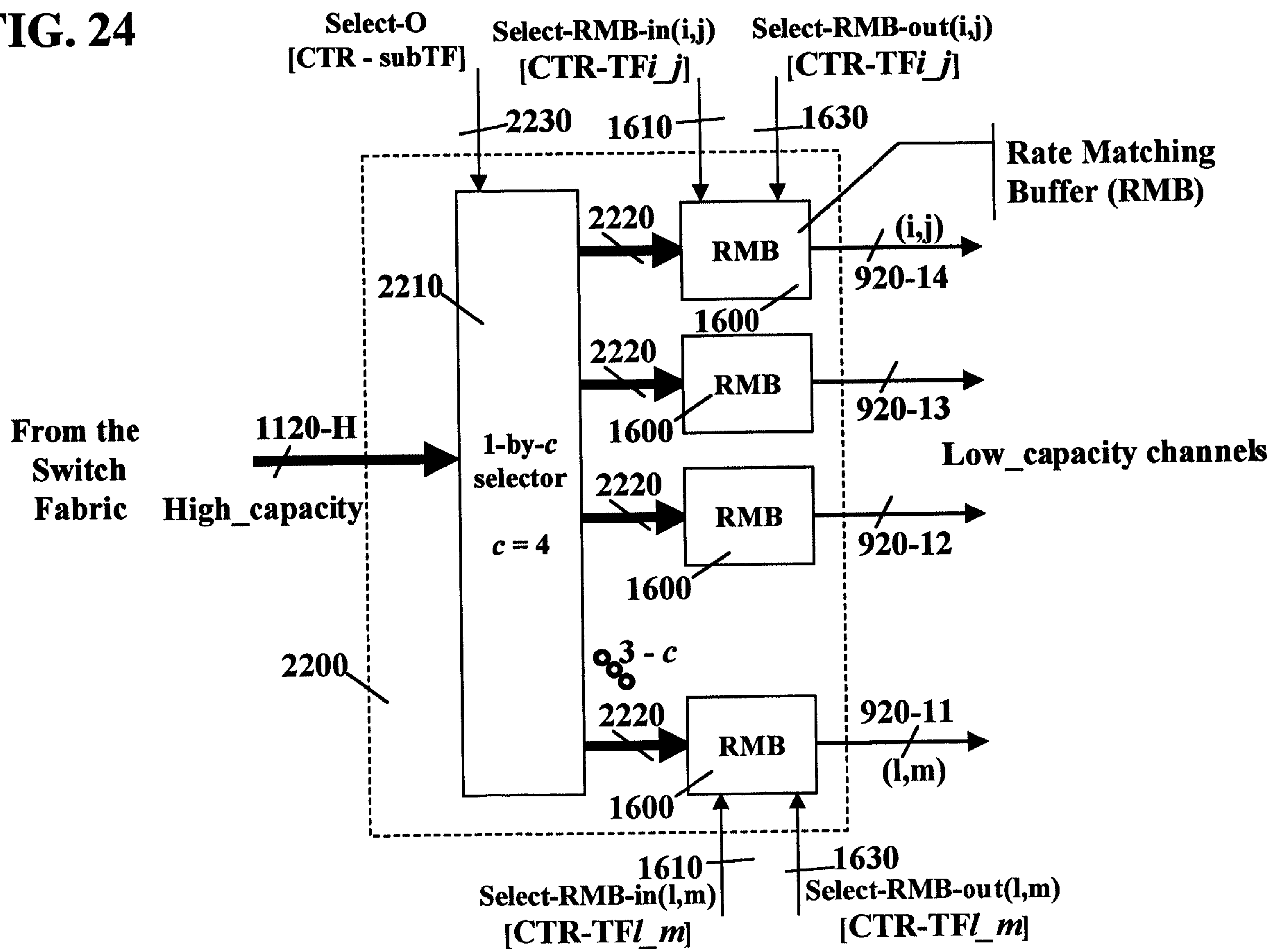
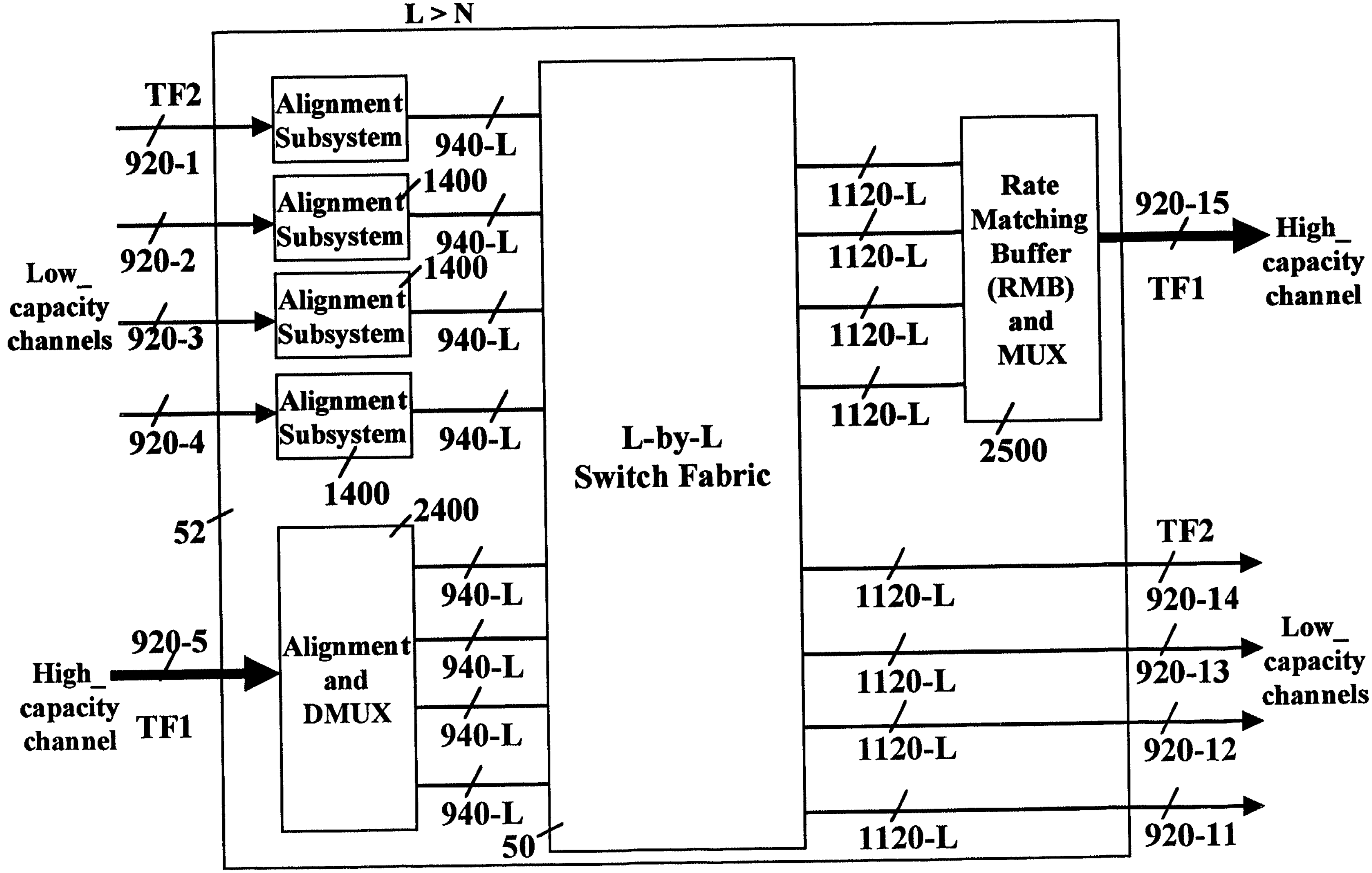

From the Switch Fabric
High_capacity
1120-H
Select-O
[CTR - subTF]
2230
Select-RMB-in(i,j)
[CTR-TFi_j]
1610
Select-RMB-out(i,j)
[CTR-TFi_j]
1630
Rate Matching Buffer (RMB)
2210
1-by-c selector
c = 4
2220
RMB
1600
(i,j)
920-14
920-13
920-12
Low_capacity channels
3 - c
2200
920-11
(l,m)
1610
Select-RMB-in(l,m)
[CTR-TFl_m]
1630
Select-RMB-out(l,m)
[CTR-TFl_m]

FIG. 25

N: number of input/output channels. E.g., N=256

L • Low_capacity = N_high • High_capacity + N_low • Low_capacity

L > N



Time Driven Switch

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FIG. 26

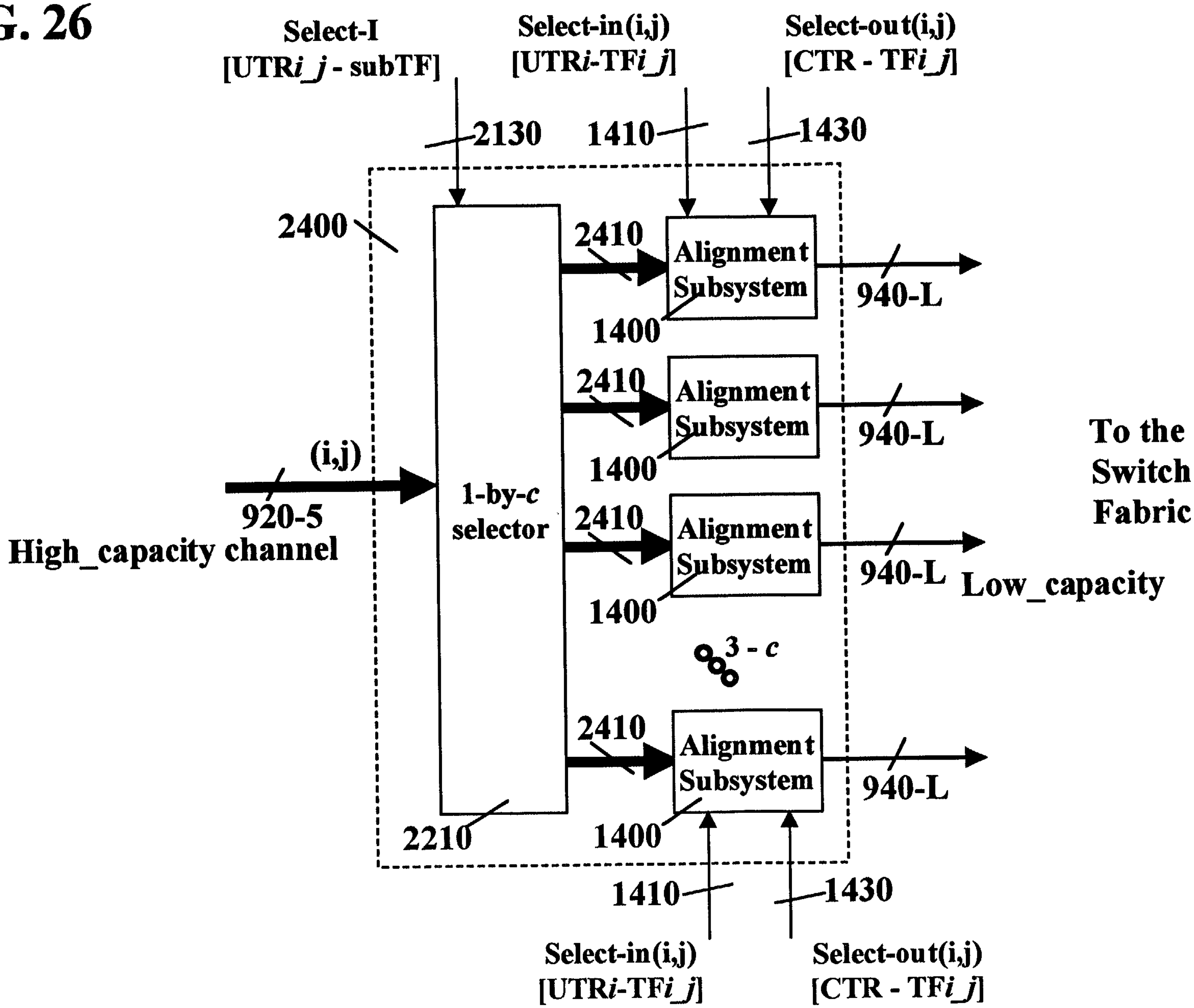

Select-I
[UTRi_j - subTF]
Select-in(i,j)
[UTRi-TFi_j]
Select-out(i,j)
[CTR - TFi_j]
2130
1410
1430
2400
2410
Alignment Subsystem
1400
940-L
(i,j)
920-5
High_capacity channel
1-by-c selector
To the Switch Fabric
Low_capacity
3 - c
2210

FIG. 27

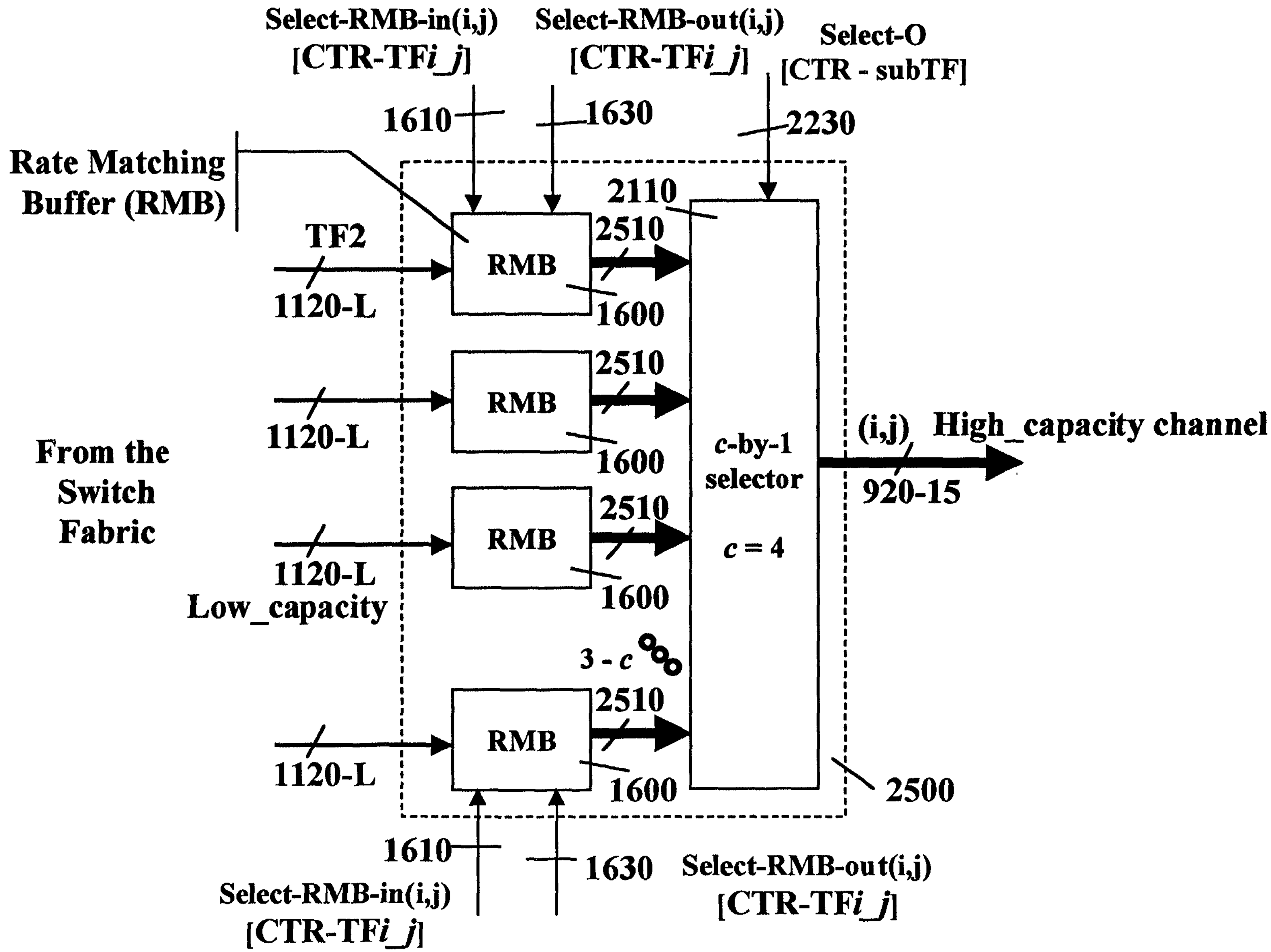
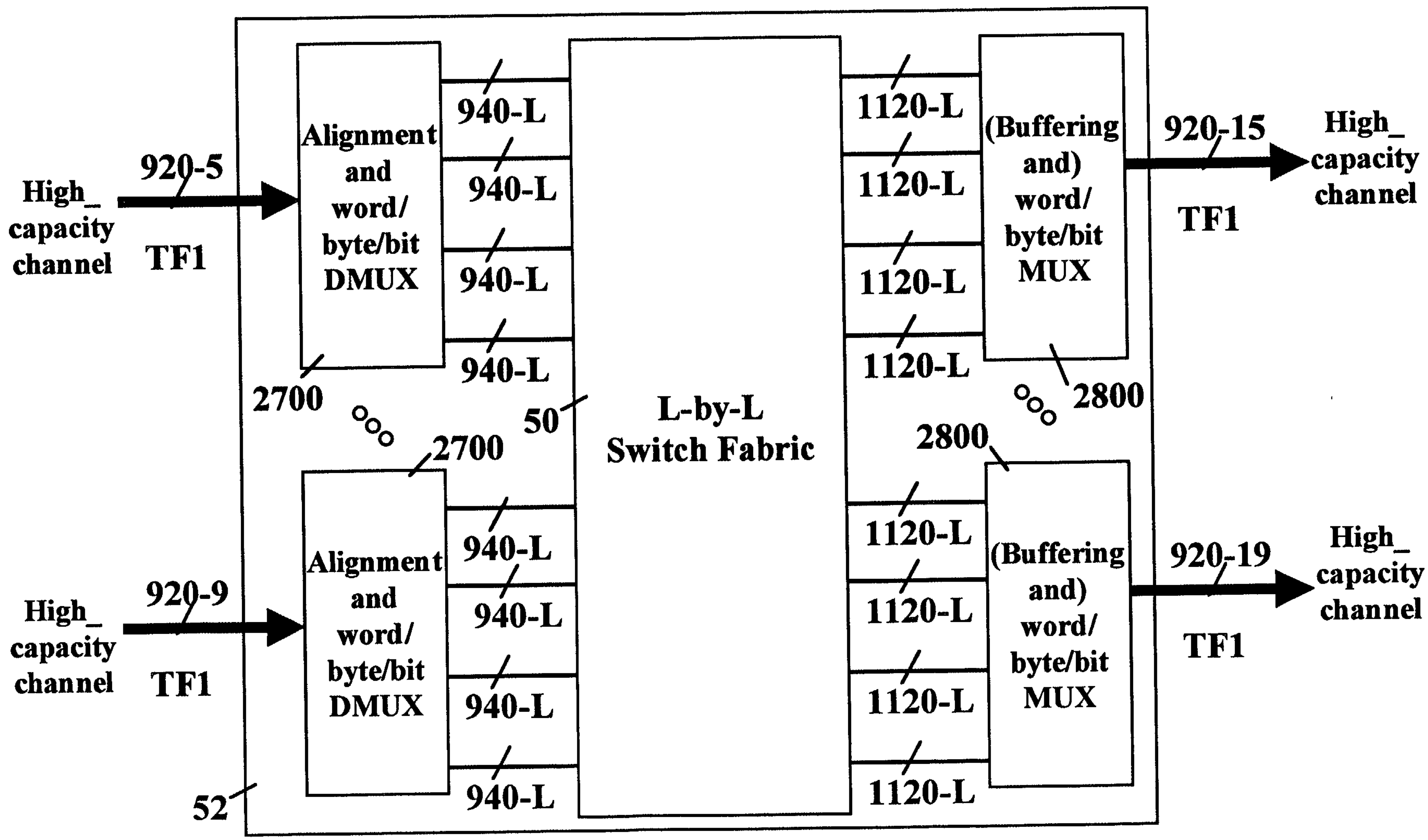

Select-RMB-in(i,j)
[CTR-TFi_j]
Select-RMB-out(i,j)
[CTR-TFi_j]
Select-O
[CTR - subTF]
1610
1630
2230
Rate Matching
Buffer (RMB)
2110
TF2
RMB
2510
1120-L
1600
From the
Switch
Fabric
c-by-1
selector
c = 4
(i,j) High_capacity channel
920-15
Low_capacity
3 - c
2500
Select-RMB-in(i,j)
[CTR-TFi_j]
Select-RMB-out(i,j)
[CTR-TFi_j]

FIG. 28

N: number of input/output channels. E.g., N=256
L • Low_capacity = N • High_capacity
L = c • N > N



Time Driven Switch

TOTZ60"ZZS09660

FIG. 29

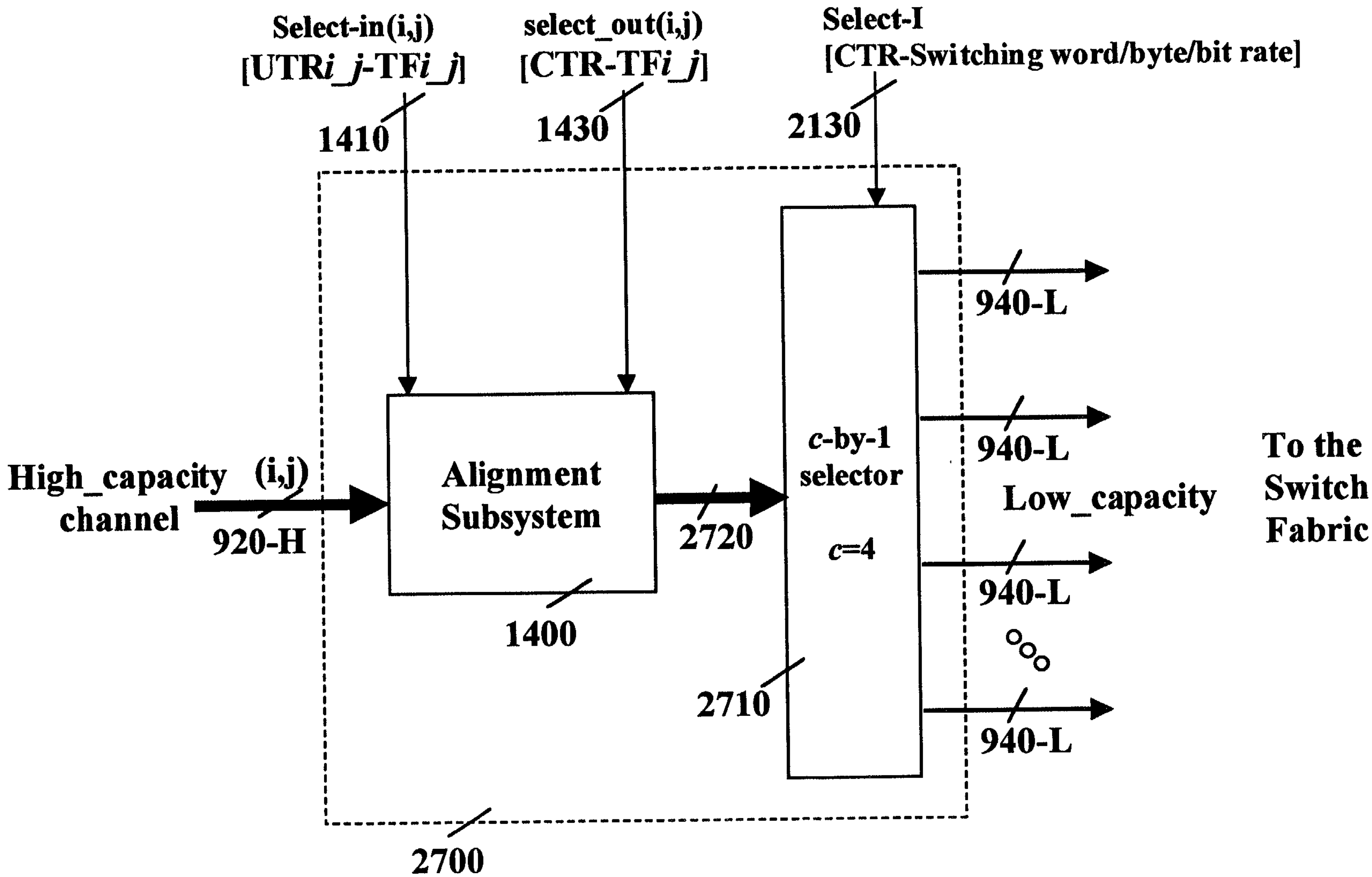
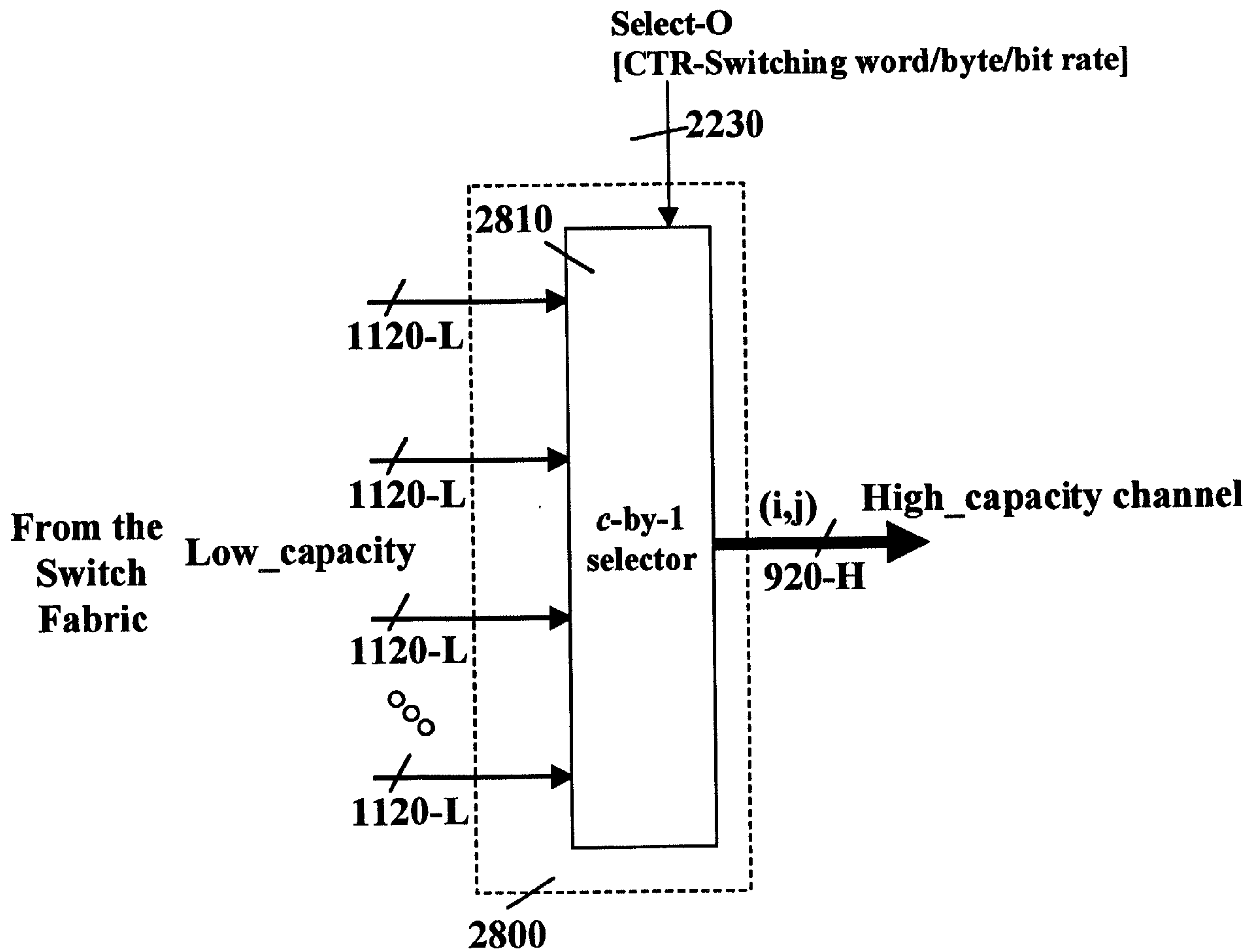


FIG. 30



Select-O
[CTR-Switching word/byte/bit rate]
2230
2810
From the Switch Fabric
Low_capacity
1120-L
1120-L
1120-L
1120-L
c-by-1 selector
(i,j)
High_capacity channel
920-H
2800

FIG. 31

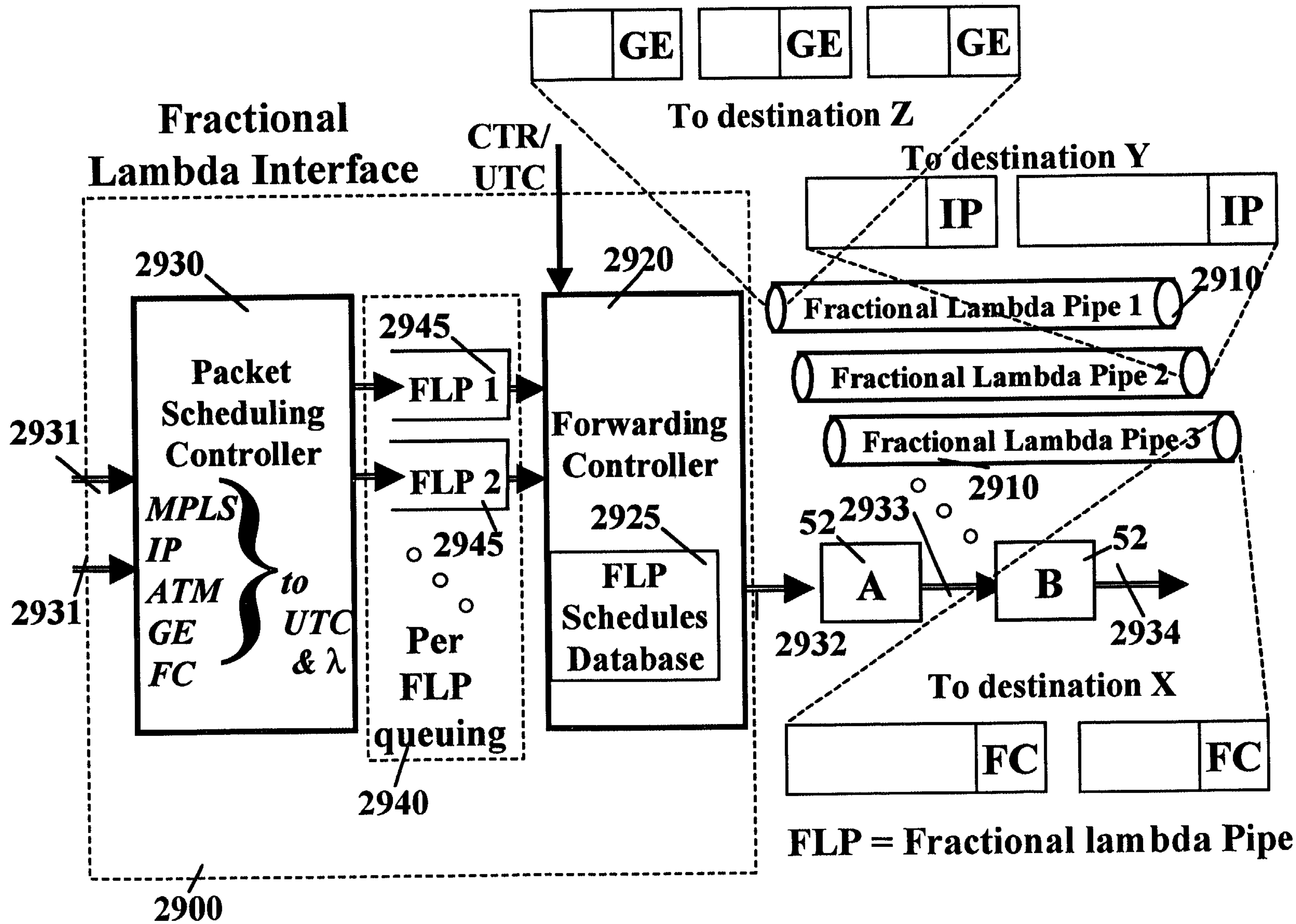

Fractional
Lambda Interface
2930
Packet
Scheduling
Controller
MPLS
IP
ATM
GE
FC
to
UTC
& λ
2931
2931
2945
FLP 1
FLP 2
2945
Per
FLP
queuing
2940
CTR/
UTC
2920
Forwarding
Controller
2925
FLP
Schedules
Database
2900
GE
GE
GE
To destination Z
To destination Y
IP
IP
Fractional Lambda Pipe 1
Fractional Lambda Pipe 2
Fractional Lambda Pipe 3
2910
2910
52
2933
A
B
52
2932
2934
To destination X
FC
FC
FLP = Fractional lambda Pipe

FIG. 32

Channel Capacity		TF Duration	TF Size		STS-1s	TFs/s
51.84	STS- 1	250	1620	1512	2	4000
		500	3240	3024	4	2000
		1000	6480	6048	8	1000
155.52	STS- 3	125	2430	2268	3	8000
		250	4860	4536	6	4000
		500	9720	9072	12	2000
622.08	STS- 12	62.5	4860	4536	6	16000
		125	9720	9072	12	8000
		250	19440	18144	24	4000
2488.32	STS- 48	62.5	19440	18144	24	16000
		31.25	9720	9072	12	32000
		15.625	4860	4536	6	64000
9953.28	STS- 192	7.8125	9720	9072	12	128000
		15.625	19440	18144	24	64000
1000	GE	125	15625	15625	19.3	8000
		100	12500	12500	15.4	10000
		80	10000	10000	12.3	12500
10000	10GE	15.625	19531.25	19531.3	24.1	64000
		12.5	15625	15625	19.3	80000
		10	12500	12500	15.4	100000

FIG. 33

Ch Capacity		TF Dur.	TF Size	GE TFs	TFs/s
1000	GE	80	10000	1.0	12500
51.84	STS- 1	250	1512	0.15	4000
		500	3024	0.30	2000
		1000	6048	0.60	1000
155.5	STS- 3	125	2268	0.23	8000
		250	4536	0.45	4000
		500	9072	0.91	2000
622.1	STS- 12	62.5	4536	0.45	16000
		125	9072	0.91	8000
		250	18144	1.81	4000
2488	STS- 48	62.5	18144	1.81	16000
		31.25	9072	0.91	32000
		15.625	4536	0.45	64000
9953	STS- 192	7.8125	9072	0.91	128000
		15.625	18144	1.81	64000
10000	10GE	8	10000	1.00	125000
		16	20000	2.00	62500

FIG. 34

Ch Capacity		TF Dur.	TF Size	GE TFs	TFs/s
1000	**GE**	**62.5**	**7812.5**	**1.0**	**16000**
51.84	STS- 1	250	1512	0.19	4000
		500	3024	0.39	2000
		1000	6048	0.77	1000
155.52	STS- 3	125	2268	0.29	8000
		250	4536	0.58	4000
		500	9072	1.16	2000
622.08	STS- 12	62.5	4536	0.58	16000
		125	9072	1.16	8000
		250	18144	2.32	4000
2488.32	STS- 48	62.5	18144	2.32	16000
		31.25	9072	1.16	32000
		15.625	4536	0.58	64000
9953.28	STS- 192	7.8125	9072	1.16	128000
		15.625	18144	2.32	64000
10000	10GE	12.5	15625	2.00	80000
		25	31250	4.00	40000

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FIG. 35

TF Alignment of UTR(j) *to* UTC - with three input queues - principle of operation:

The same queue is not used simultaneously for:

1. Receiving data packets from the serial link, and
2. Forwarding data packets to the switch

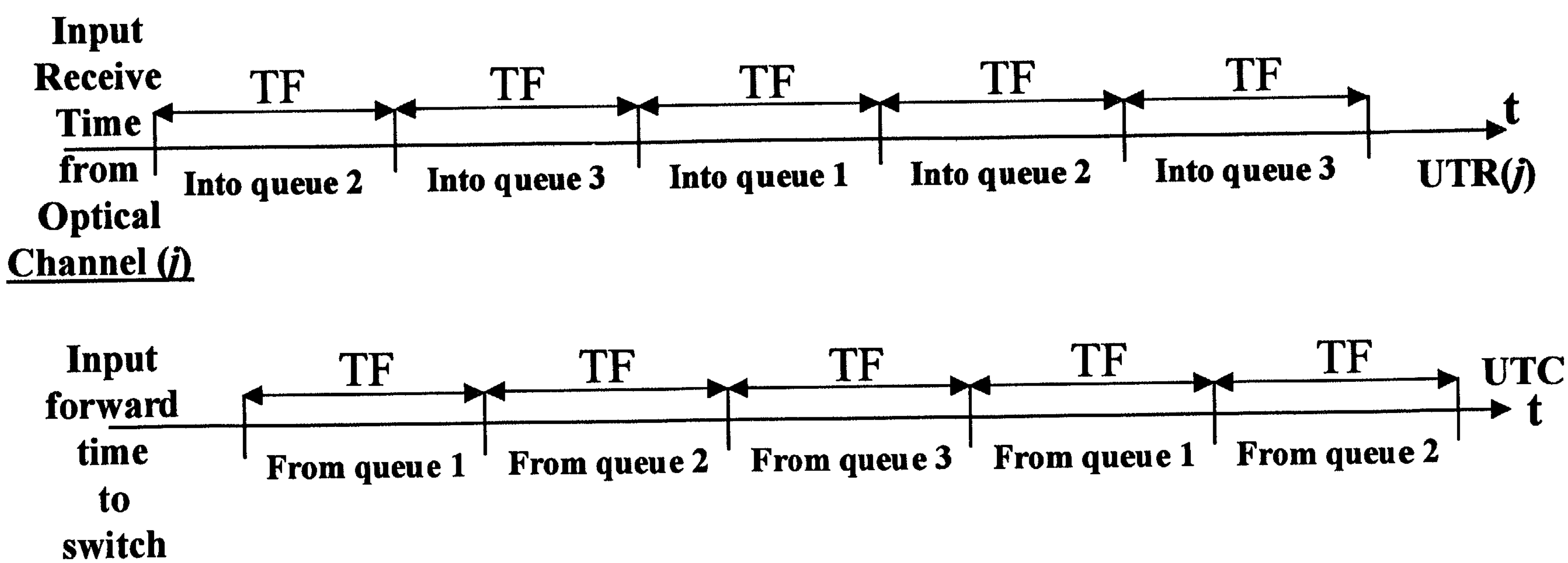
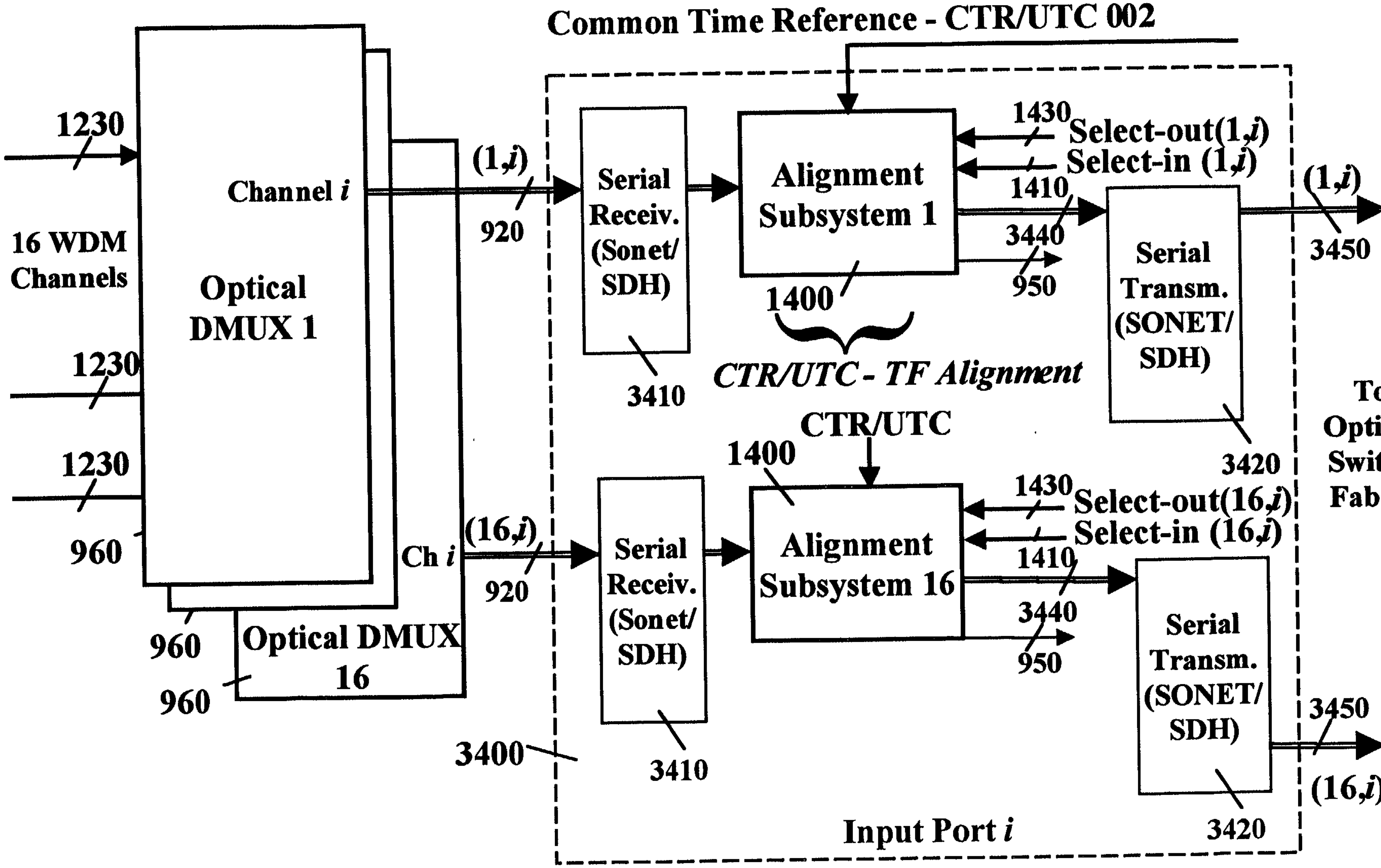


FIG. 36



Common Time Reference - CTR/UTC 002
1230
16 WDM Channels
1230
1230
960
960
960
Optical DMUX 1
Channel i
Optical DMUX 16
Ch i
(1,i)
920
(16,i)
920
Serial Receiv. (Sonet/ SDH)
3410
Alignment Subsystem 1
1400
CTR/UTC - TF Alignment
CTR/UTC
1400
Alignment Subsystem 16
1430
Select-out(1,i)
Select-in (1,i)
1410
3440
950
1430
Select-out(16,i)
Select-in (16,i)
Serial Transm. (SONET/ SDH)
3420
(1,i)
3450
(16,i)
To Optical Switch Fabric
3400
Input Port i

FIG. 37

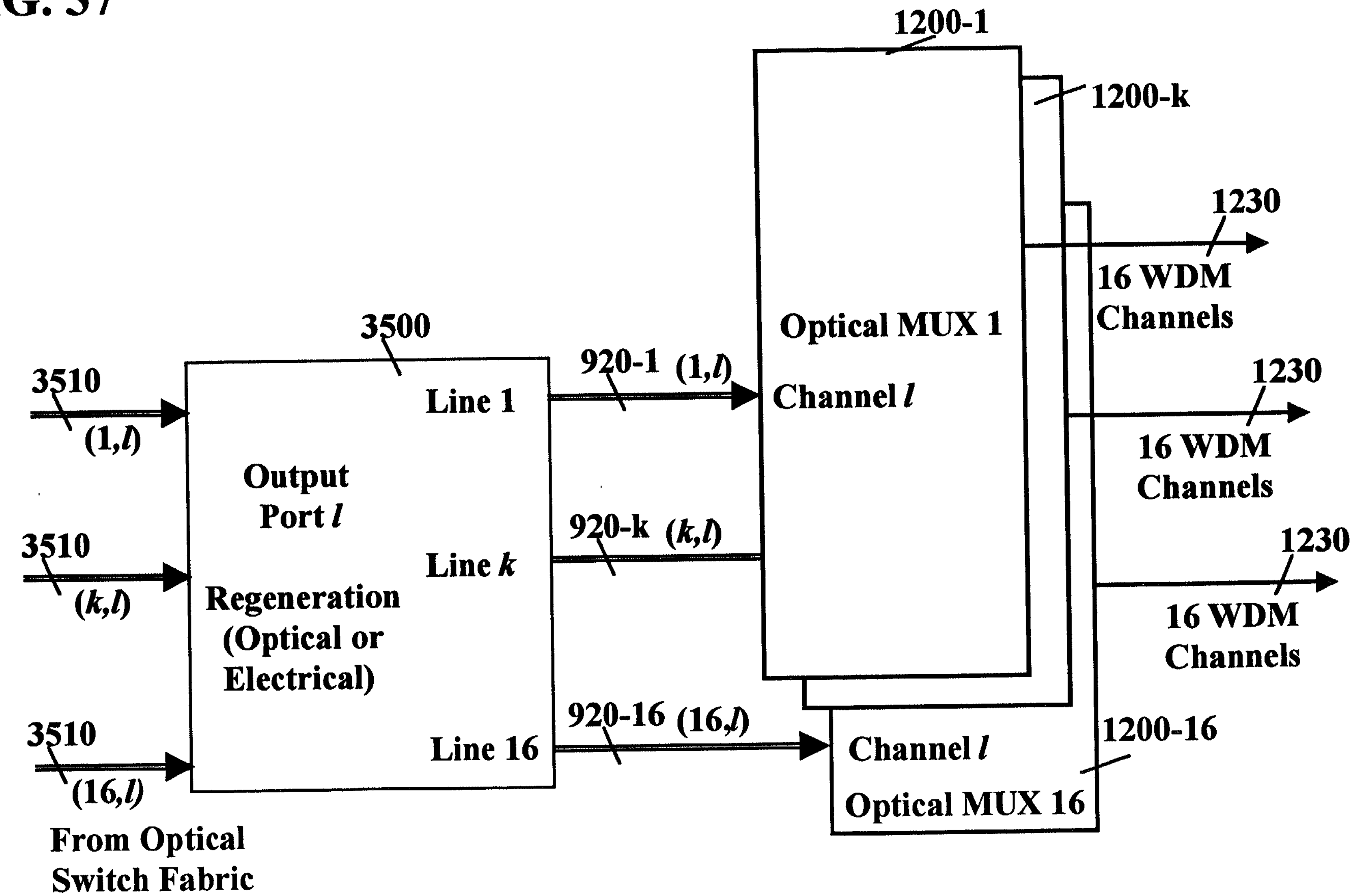
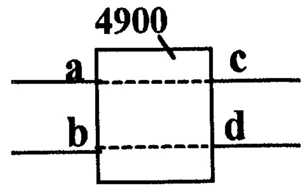

3510
(1,*l*)
3510
(*k*,*l*)
3510
(16,*l*)
From Optical Switch Fabric
3500
Output Port *l*
Regeneration (Optical or Electrical)
Line 1
Line *k*
Line 16
920-1 (1,*l*)
920-k (*k*,*l*)
920-16 (16,*l*)
1200-1
Optical MUX 1
Channel *l*
1200-k
1200-16
Channel *l*
Optical MUX 16
1230
16 WDM Channels
1230
16 WDM Channels
1230
16 WDM Channels

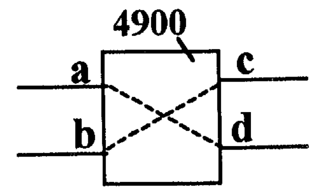
FIG. 38

(A)



Straight Connection of a
2-by-2 Optical Switching Block

(B)



Cross Connection of a
2-by-2 Optical Switching Block

(C)

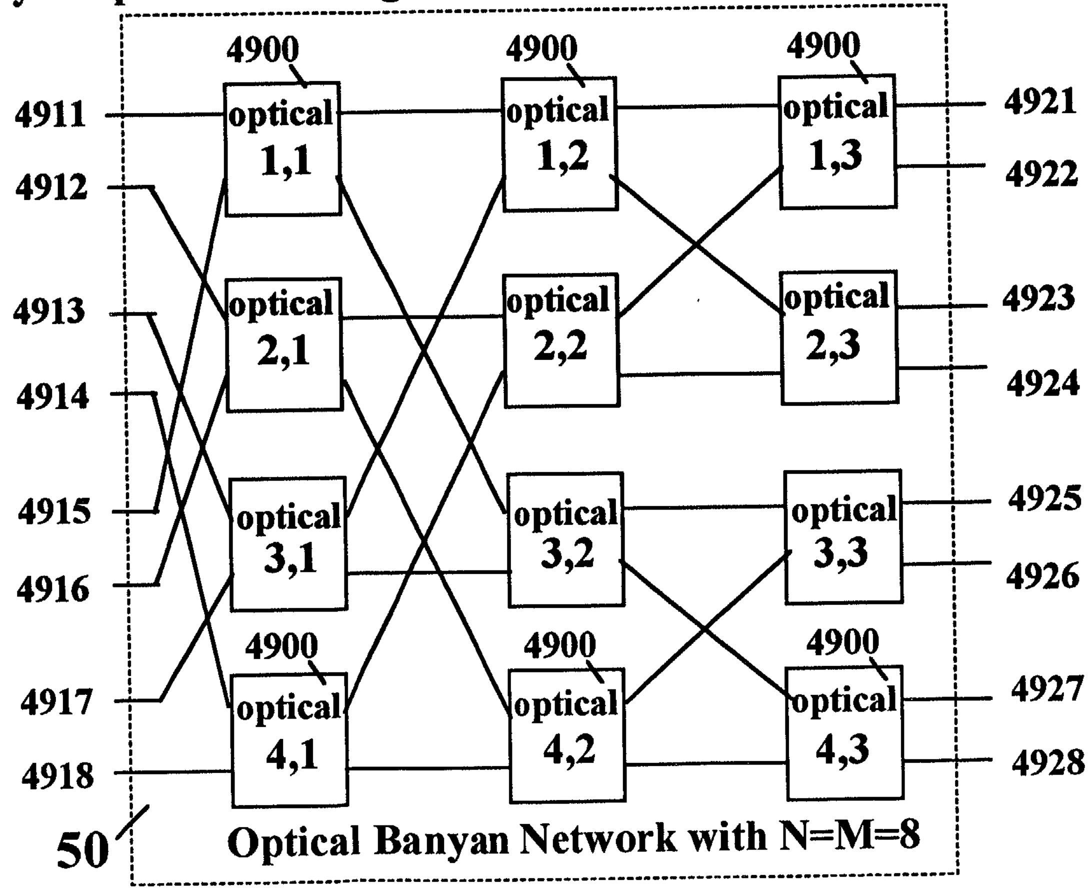


FIG. 39

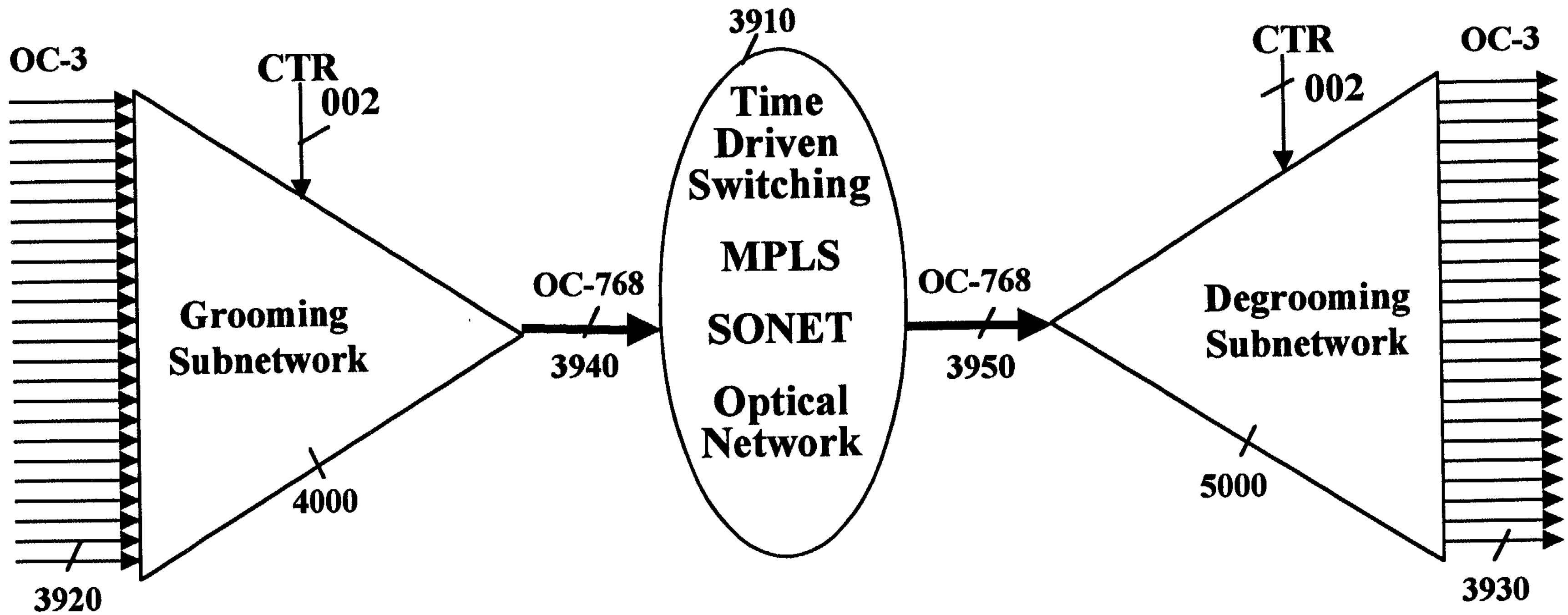

OC-3
CTR
002
Grooming
Subnetwork
4000
3920
OC-768
3940
3910
Time
Driven
Switching
MPLS
SONET
Optical
Network
OC-768
3950
CTR
002
OC-3
Degrooming
Subnetwork
5000
3930

FIG. 40

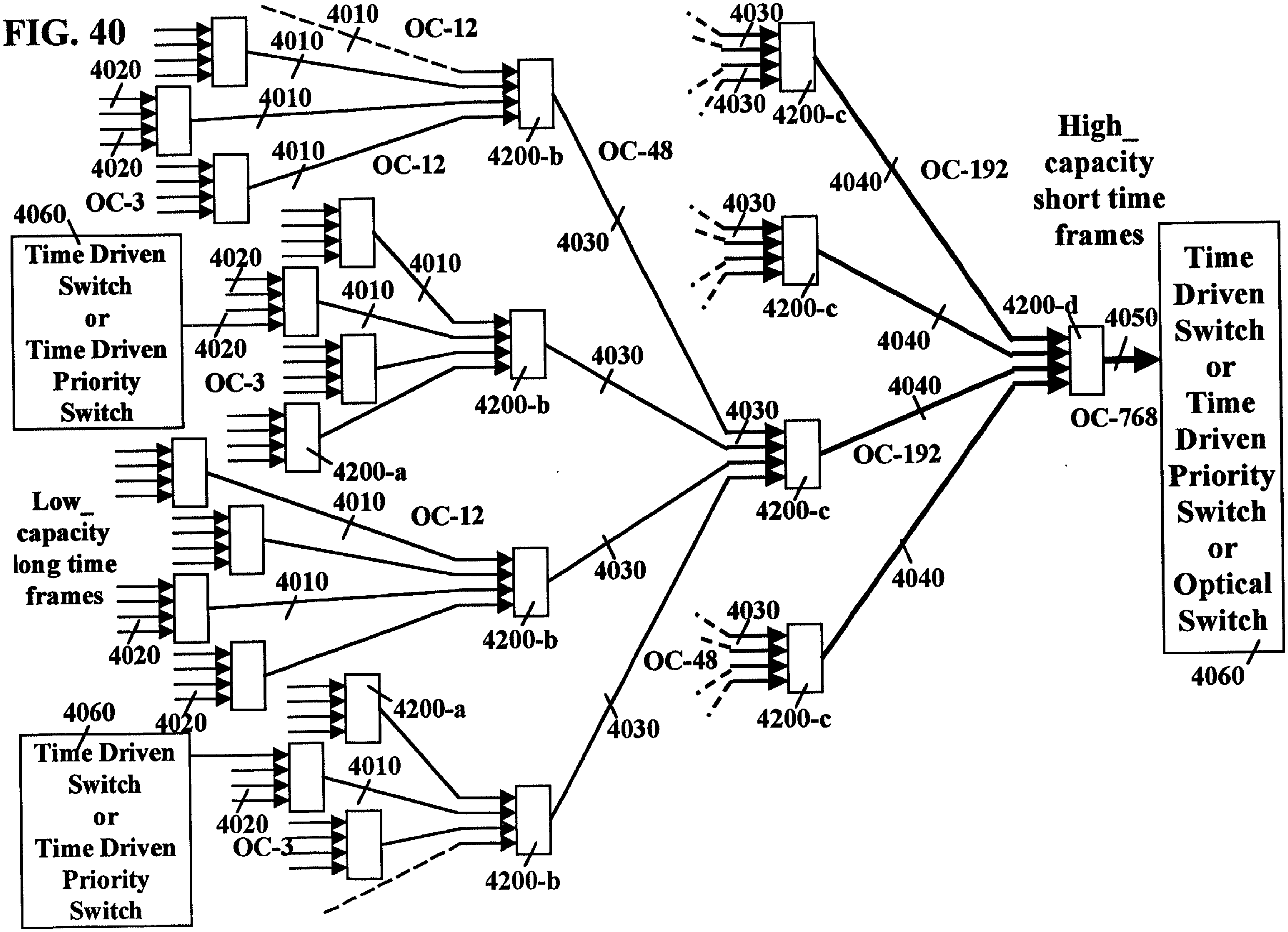

4010
4020
OC-12
OC-3
4060
Time Driven Switch or Time Driven Priority Switch
4200-a
4200-b
OC-48
4030
Low_ capacity long time frames
4200-c
OC-192
4040
High_ capacity short time frames
4200-d
4050
OC-768
Time Driven Switch or Time Driven Priority Switch or Optical Switch

FIG. 41

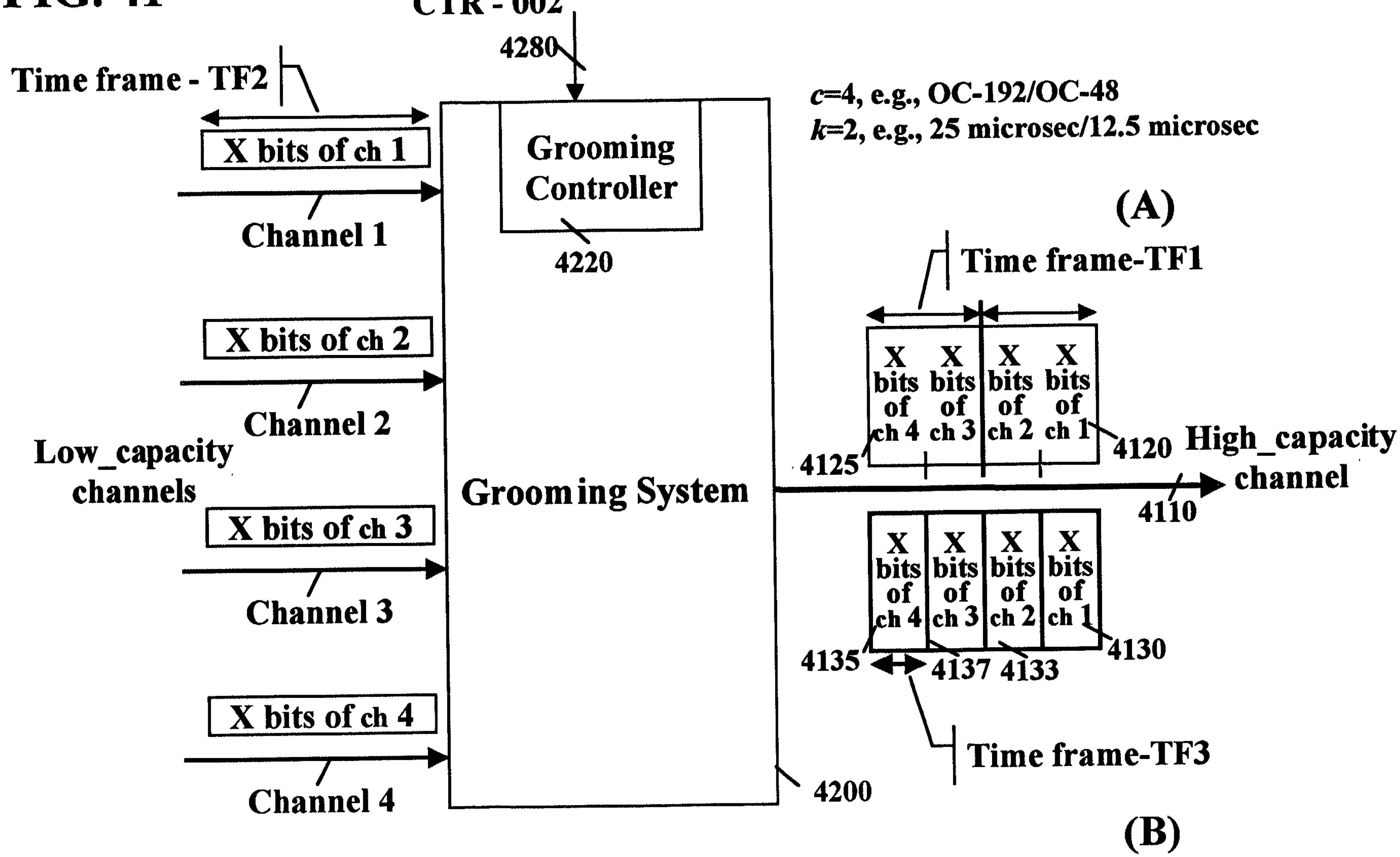


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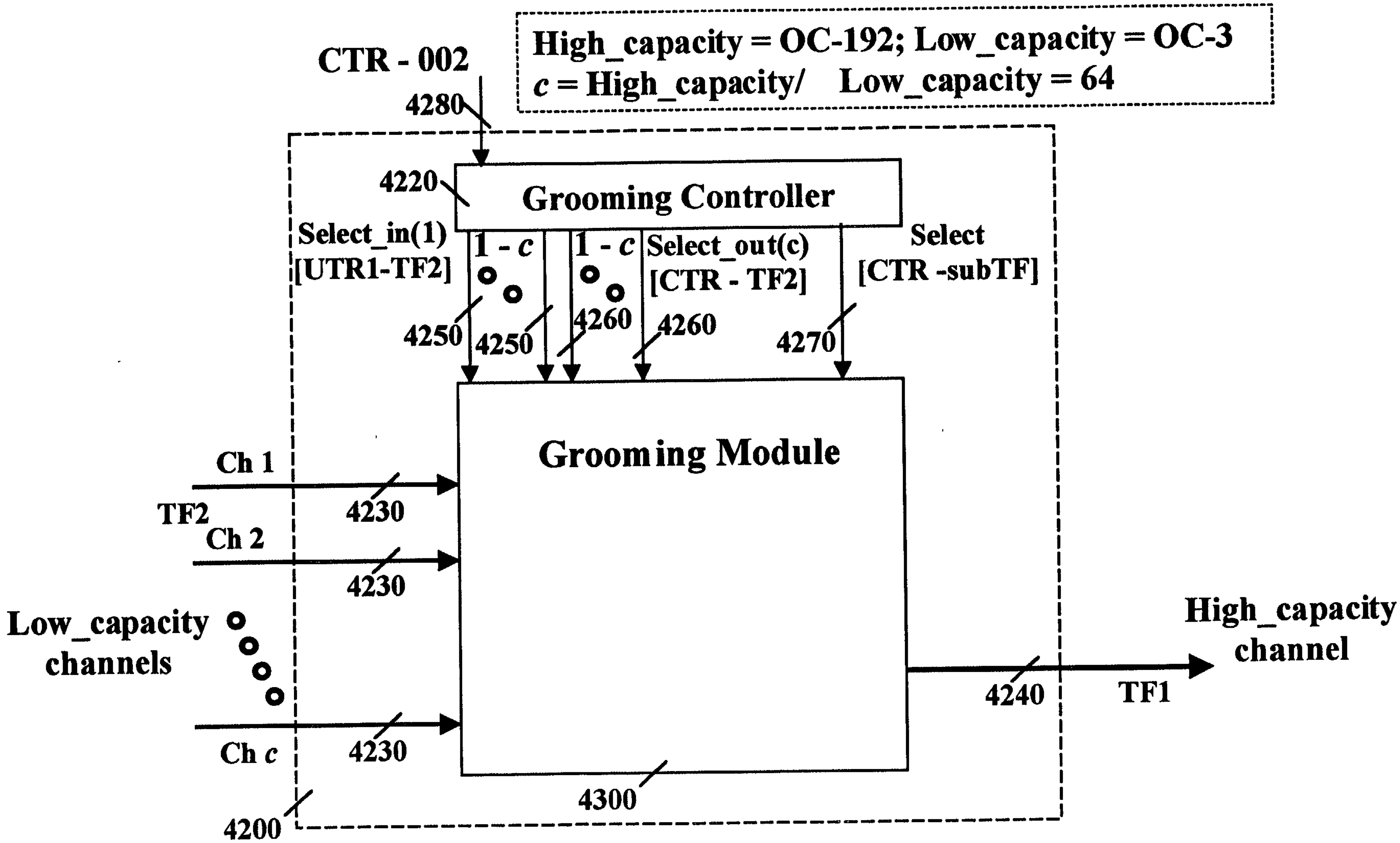
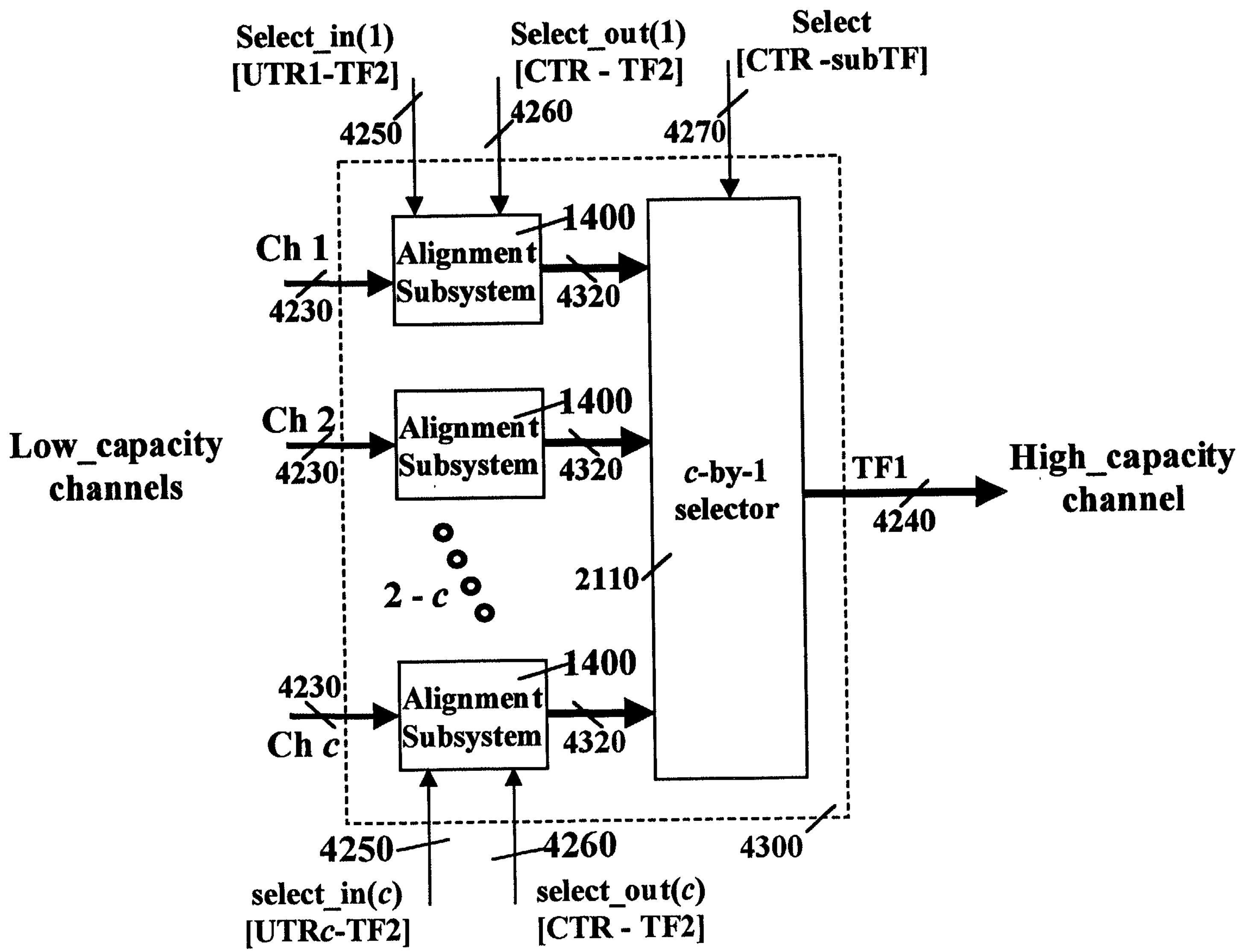
FIG. 42



High_capacity = OC-192; Low_capacity = OC-3
c = High_capacity/ Low_capacity = 64
CTR - 002
4280
4220
Grooming Controller
Select_in(1)
[UTR1-TF2]
1 - c
1 - c
Select_out(c)
[CTR - TF2]
Select
[CTR -subTF]
4250
4250
4260
4260
4270
Grooming Module
Ch 1
TF2
Ch 2
4230
4230
Low_capacity
channels
Ch c
4230
High_capacity
channel
4240
TF1
4300
4200

FIG. 43



Select_in(1)
[UTR1-TF2]
Select_out(1)
[CTR - TF2]
Select
[CTR -subTF]
4250
4260
4270
Ch 1
Alignment Subsystem
1400
4320
4230
Ch 2
Alignment Subsystem
1400
4320
4230
Low_capacity channels
c-by-1 selector
TF1
4240
High_capacity channel
2 - c
2110
4230
Ch c
Alignment Subsystem
1400
4320
4250
4260
4300
select_in(c)
[UTRc-TF2]
select_out(c)
[CTR - TF2]

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FIG. 44

- $CC1\_length \cdot TF1 = CC2\_length \cdot TF2 = CC3\_length \cdot TF2$
- $TF2 = (SC1\_length / SC2\_length) \cdot TF1 = k \cdot TF1$, where the common cycles of ***TF1*** and ***TF2*** are aligned with respect to UTC.

For $k = 2$ and $c = 4$ (e.g., High_capacity=OC-192, Low_capacity=OC-48):

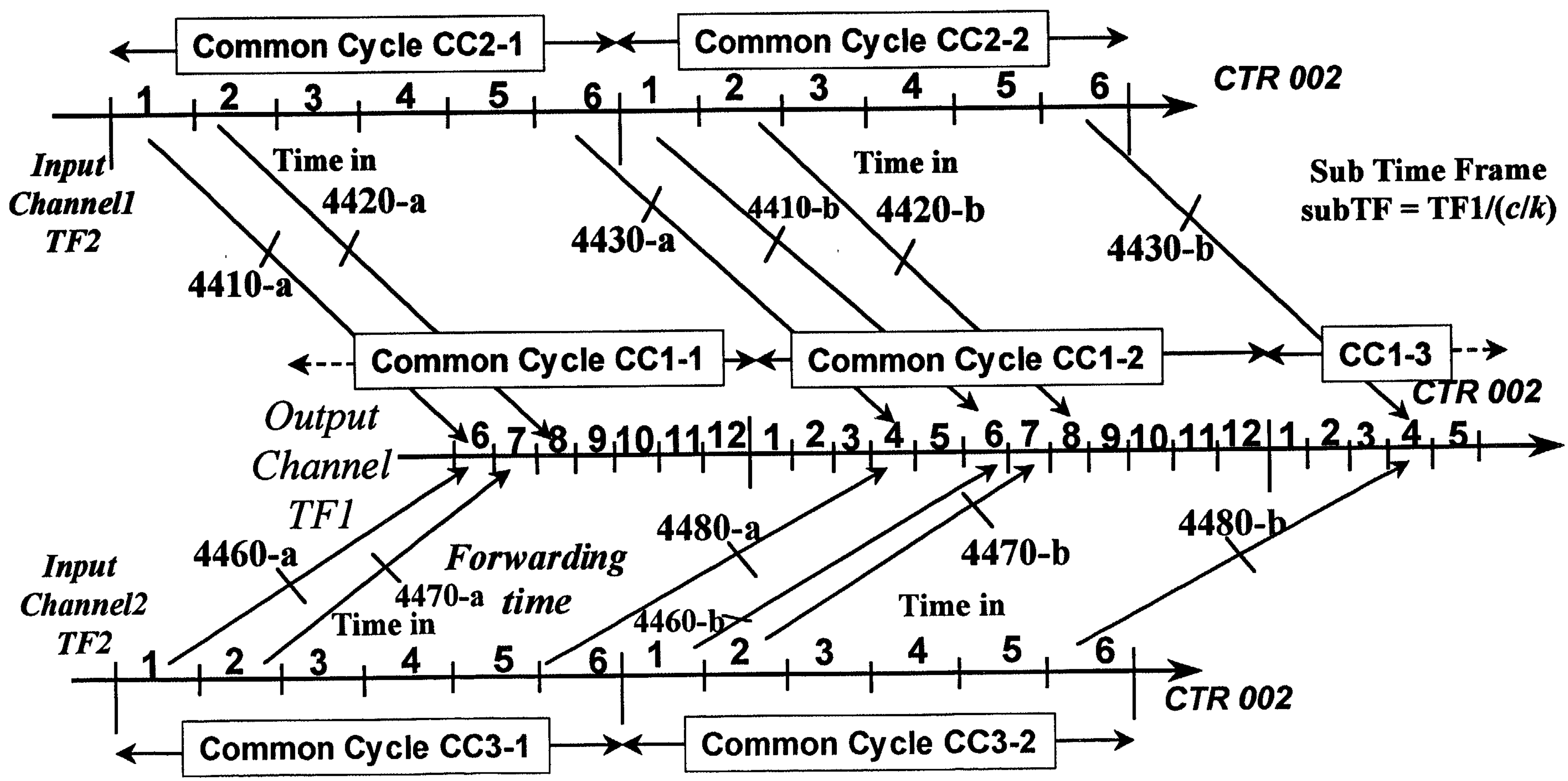
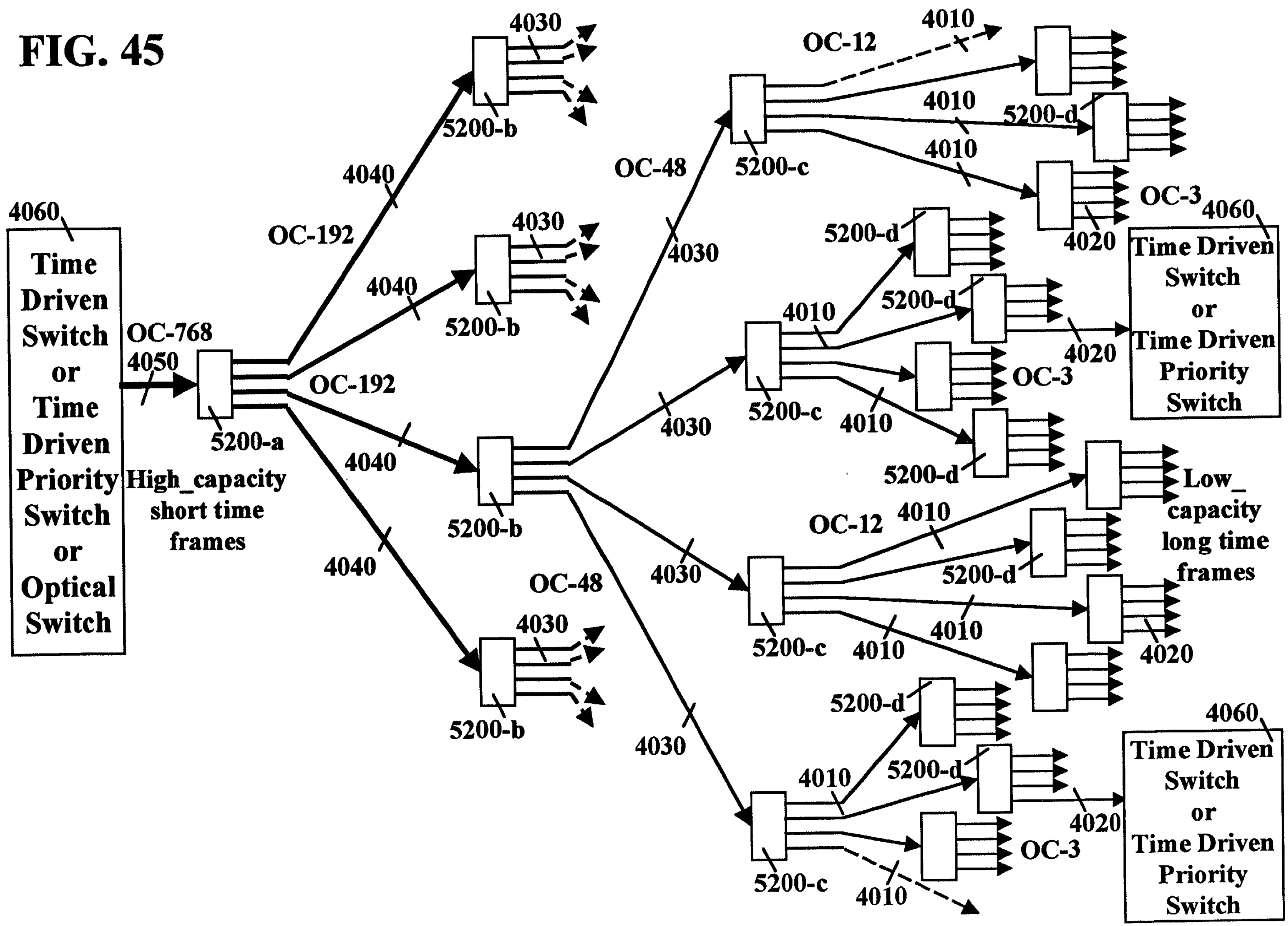
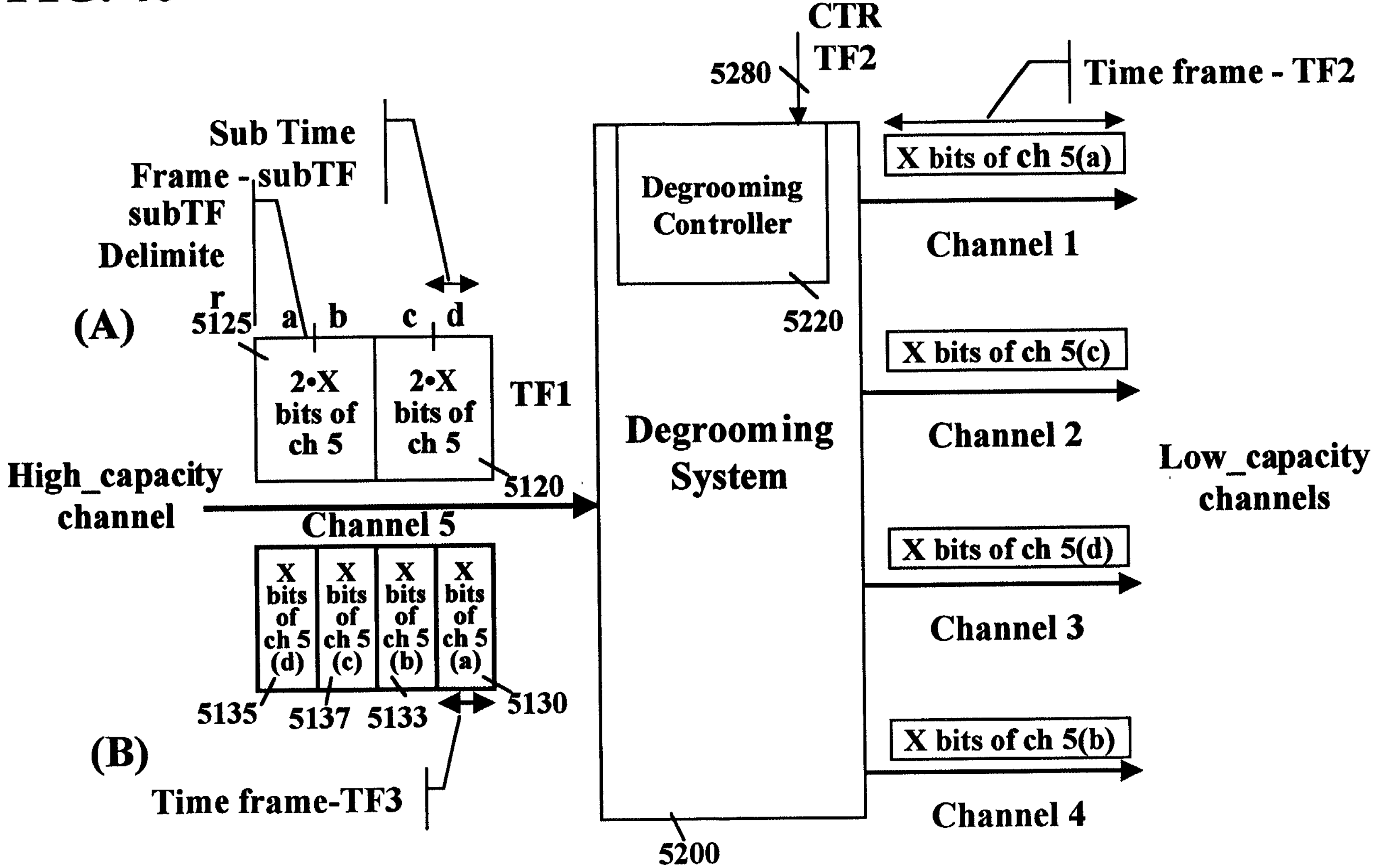


FIG. 45



Time Driven Switch or Time Driven Priority Switch or Optical Switch
4060
OC-768
4050
5200-a
High_capacity short time frames
OC-192
4040
5200-b
4030
OC-48
5200-c
OC-12
4010
5200-d
4020
OC-3
Time Driven Switch or Time Driven Priority Switch
Low_ capacity long time frames

FIG. 46



c=4, e.g., OC-192/OC-48
k=2, e.g., 25 microsec/12.5 microsec

FIG. 47

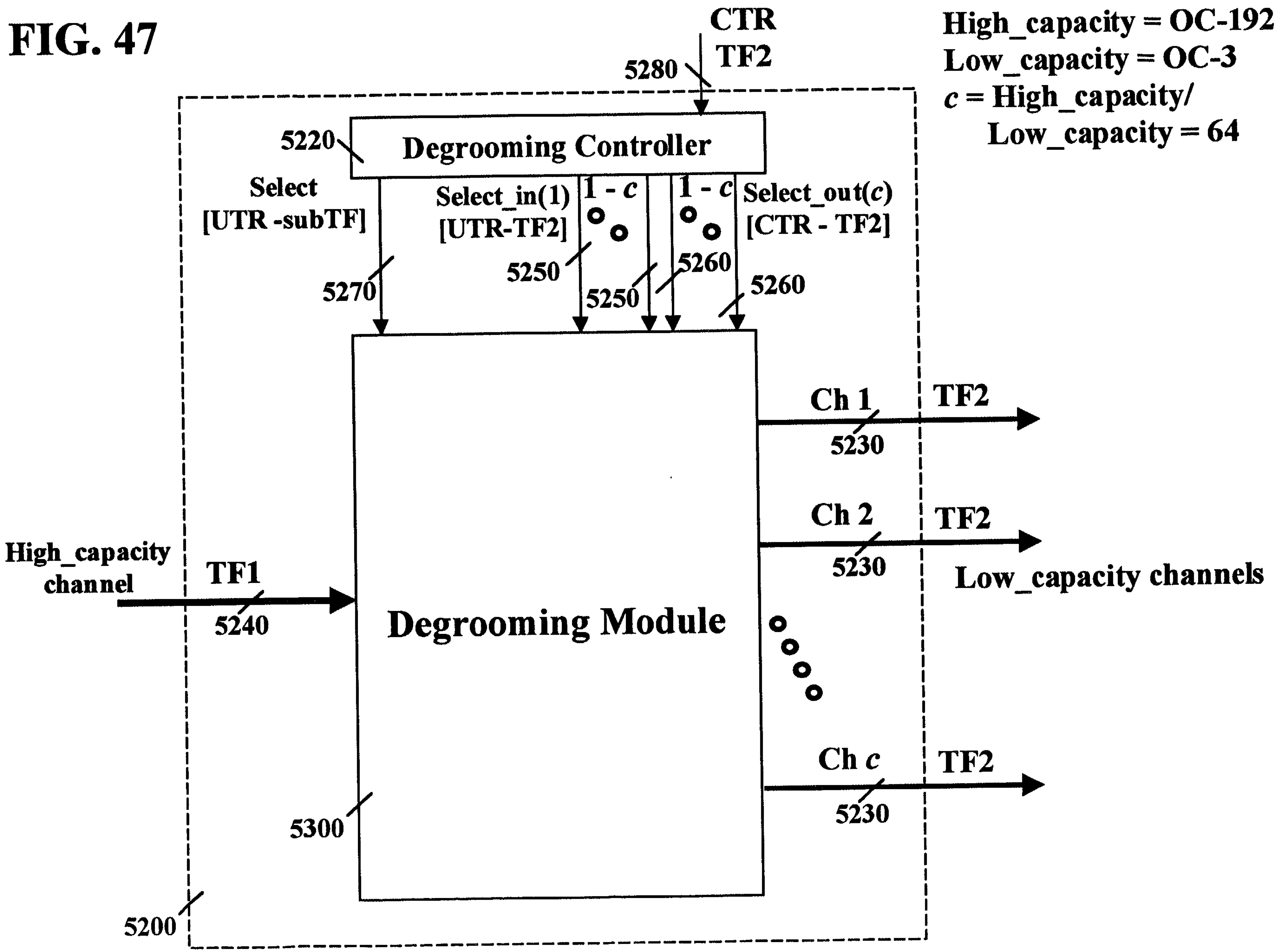

High_capacity = OC-192
Low_capacity = OC-3
c = High_capacity/ Low_capacity = 64
CTR
TF2
5280
5220
Degrooming Controller
Select
[UTR -subTF]
Select_in(1)
[UTR-TF2]
1 - c
1 - c
Select_out(c)
[CTR - TF2]
5270
5250
5250
5260
5260
High_capacity channel
TF1
5240
Degrooming Module
5300
5200
Ch 1
5230
TF2
Ch 2
5230
TF2
Low_capacity channels
Ch c
5230
TF2

FIG. 48

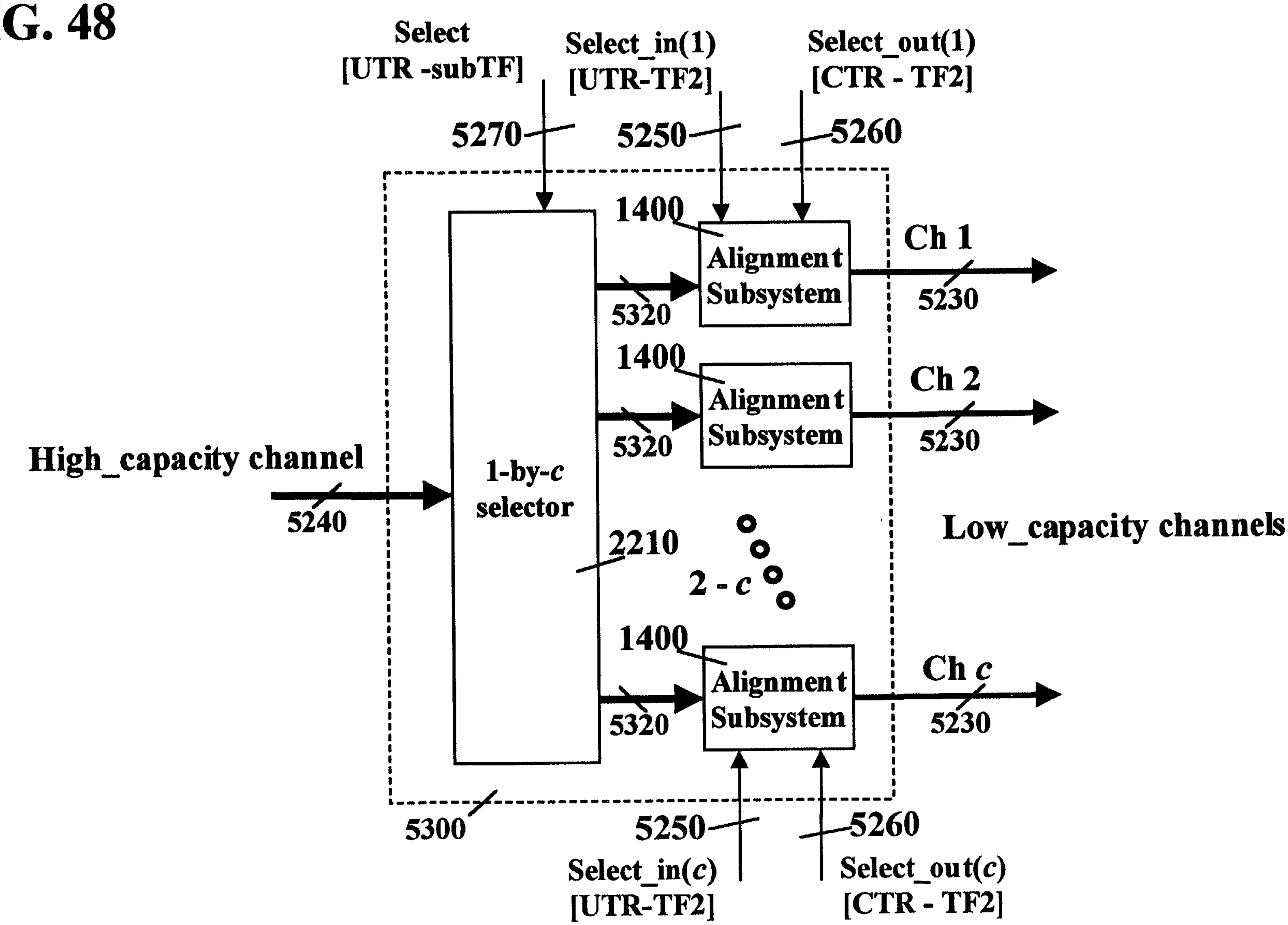

Select
[UTR -subTF]
5270
Select_in(1)
[UTR-TF2]
5250
Select_out(1)
[CTR - TF2]
5260
High_capacity channel
5240
1-by-c
selector
2210
1400
Alignment
Subsystem
5320
Ch 1
5230
Ch 2
2 - c
Ch c
Low_capacity channels
5300
5250
Select_in(c)
[UTR-TF2]
5260
Select_out(c)
[CTR - TF2]

FIG. 49

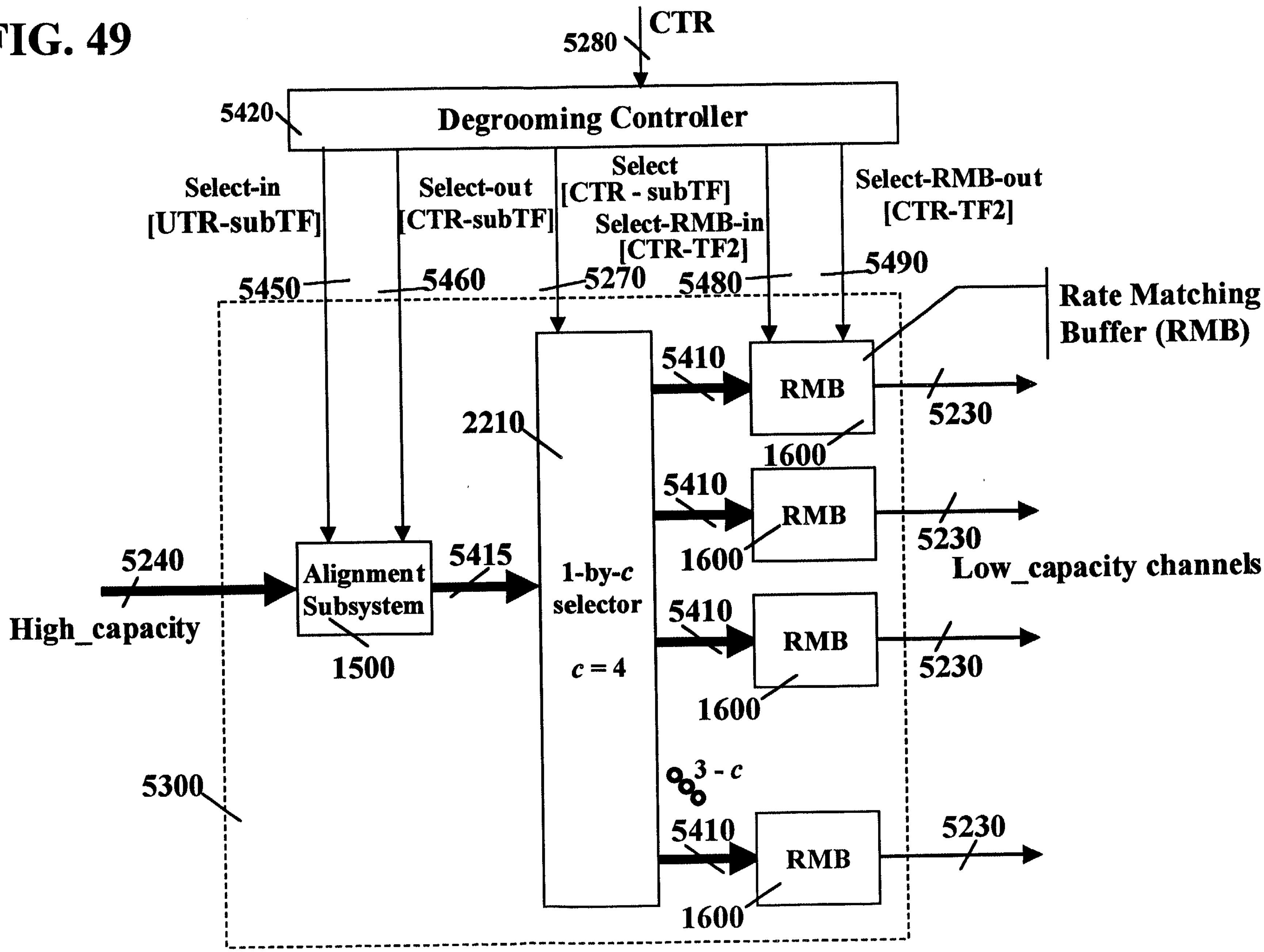
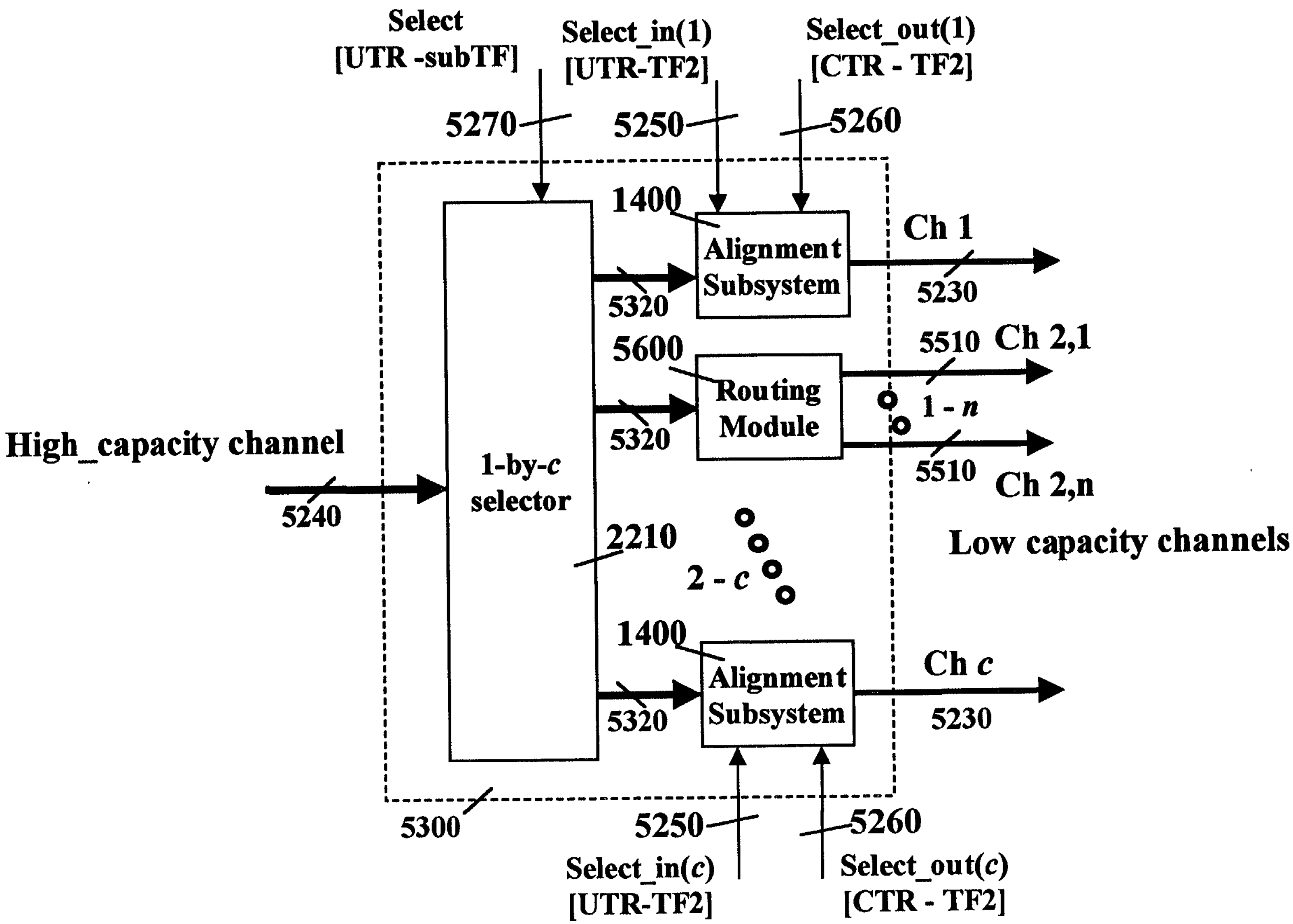

CTR
5280
5420
Degrooming Controller
Select-in
[UTR-subTF]
Select-out
[CTR-subTF]
Select
[CTR - subTF]
Select-RMB-in
[CTR-TF2]
Select-RMB-out
[CTR-TF2]
5450
5460
5270
5480
5490
Rate Matching
Buffer (RMB)
5240
High_capacity
Alignment
Subsystem
1500
5415
2210
1-by-c
selector
c = 4
5410
RMB
1600
5230
Low_capacity channels
3 - c
5300

FIG. 50



Select
[UTR -subTF]
Select_in(1)
[UTR-TF2]
Select_out(1)
[CTR - TF2]
5270
5250
5260
1400
Alignment Subsystem
Ch 1
5230
5320
5600
Routing Module
5510
Ch 2,1
1 - n
5510
Ch 2,n
High_capacity channel
5240
1-by-c selector
5320
2210
2 - c
Low capacity channels
1400
Alignment Subsystem
Ch c
5230
5320
5300
5250
5260
Select_in(c)
[UTR-TF2]
Select_out(c)
[CTR - TF2]

FIG. 51

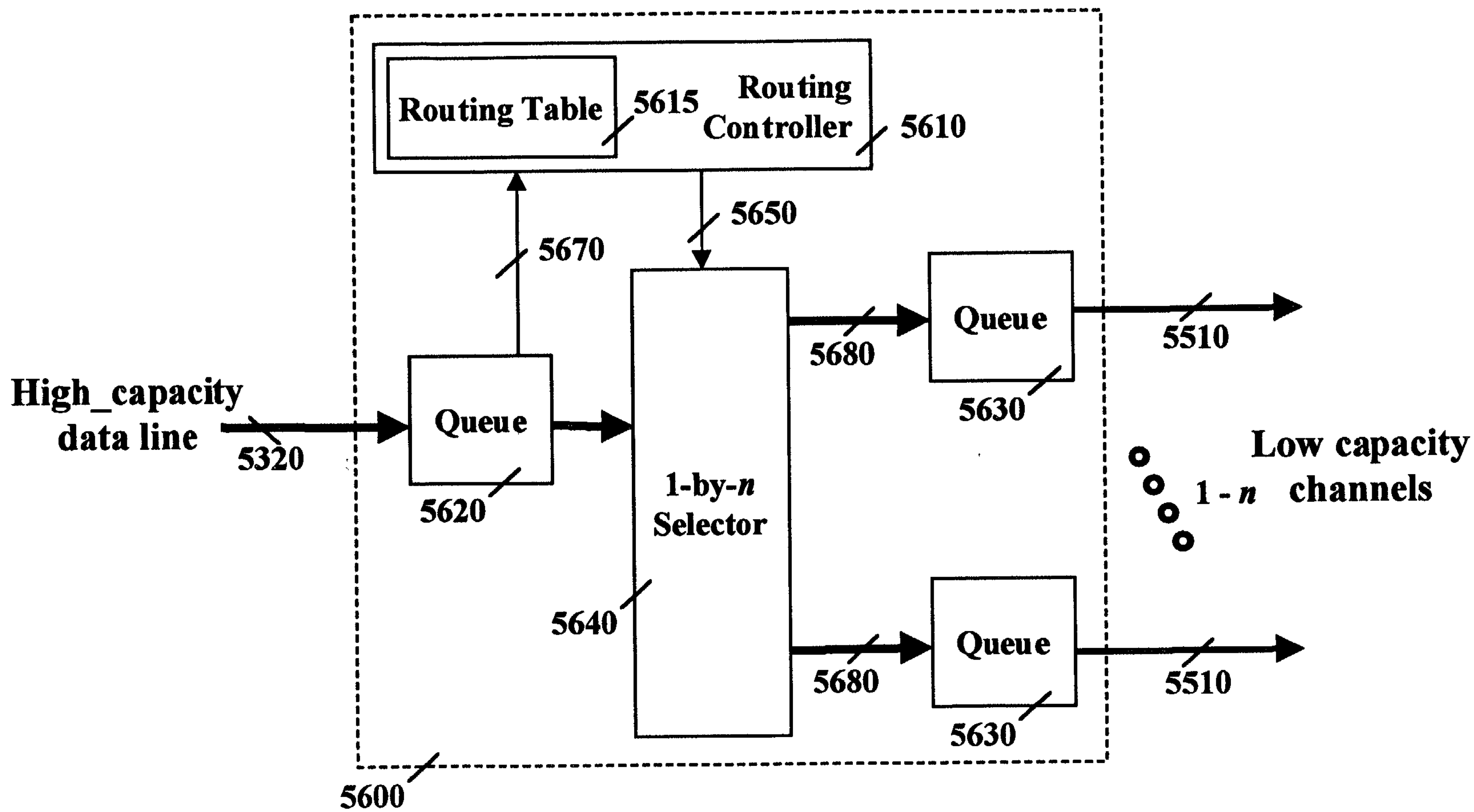


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FIG. 52

- $CC1\_length \cdot TF1 = CC2\_length \cdot TF2 = CC3\_length \cdot TF2$
- $TF2 = (SC1\_length / SC2\_length) \cdot TF1 = k \cdot TF1$, where the common cycles of $TF1$ and $TF2$ are aligned with respect to UTC.

For $k = 2$ and $c = 4$ (e.g., High_capacity=OC-192, Low_capacity=OC-48):

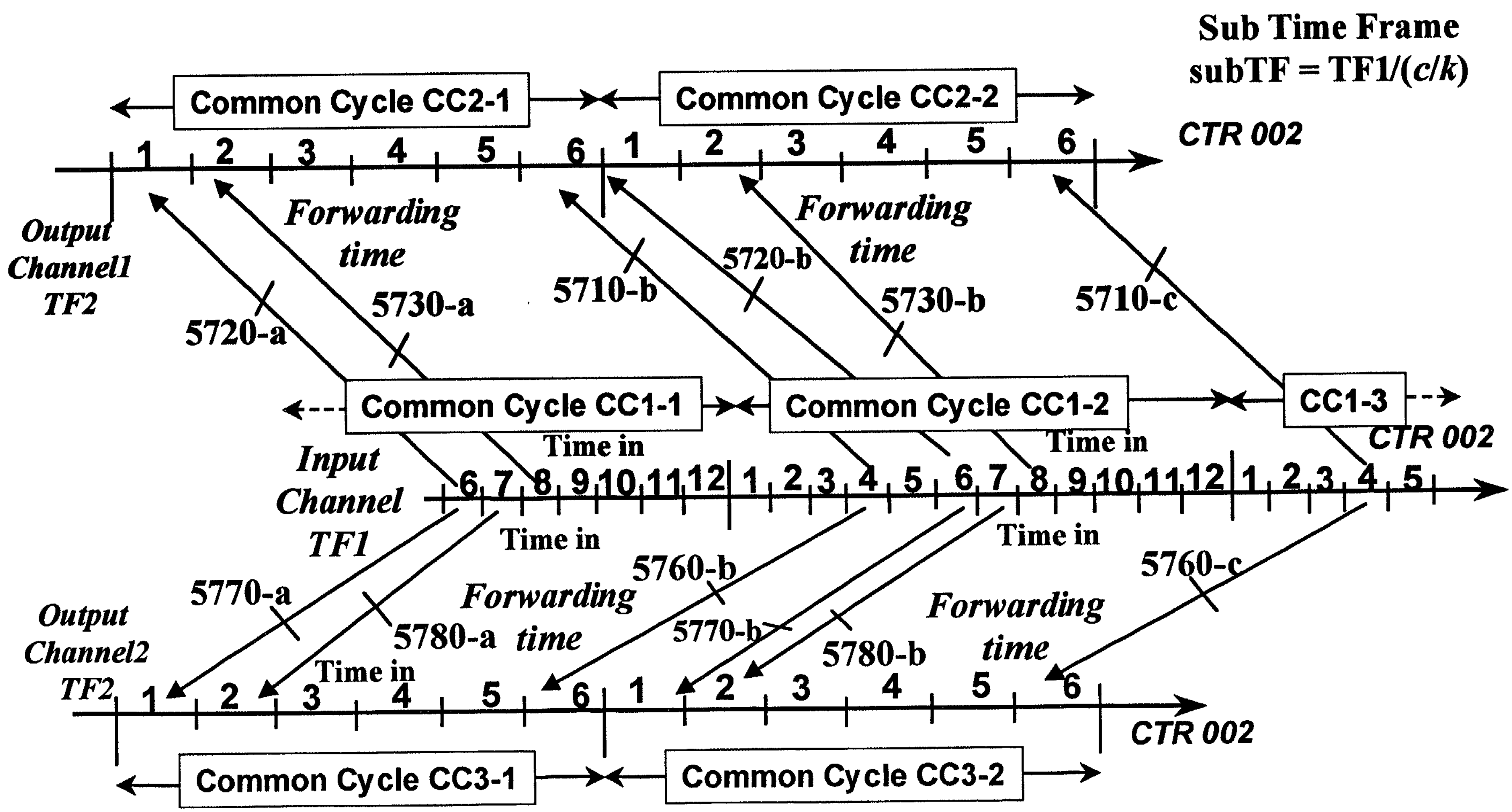

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FIG. 53

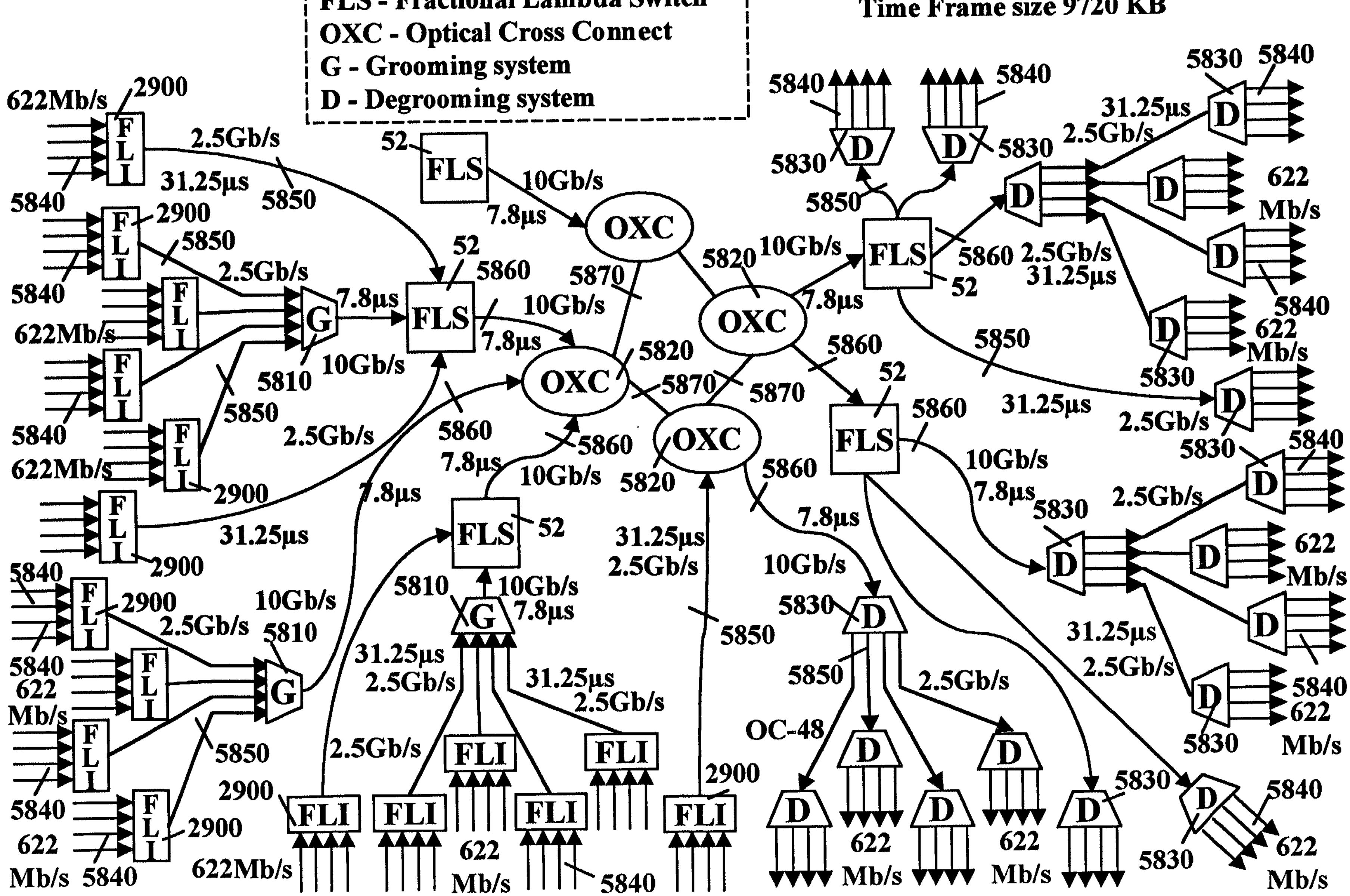

FIG. 54

FLI - Fractional Lambda Interface
FLS - Fractional Lambda Switch
OXC - Optical Cross Connect
G - Grooming system
D - Degrooming system

12 STS-1s per time frame

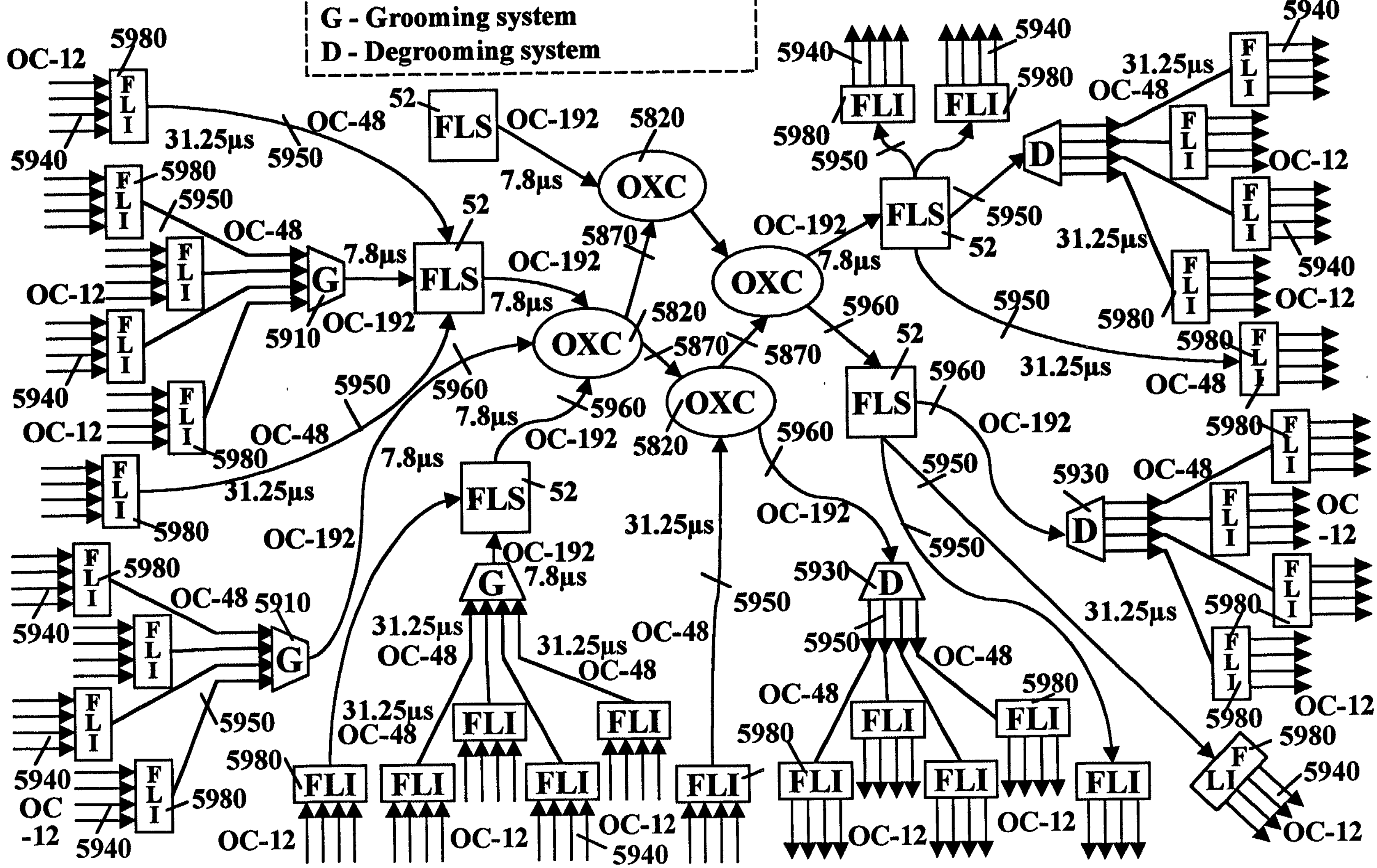

FIG. 55

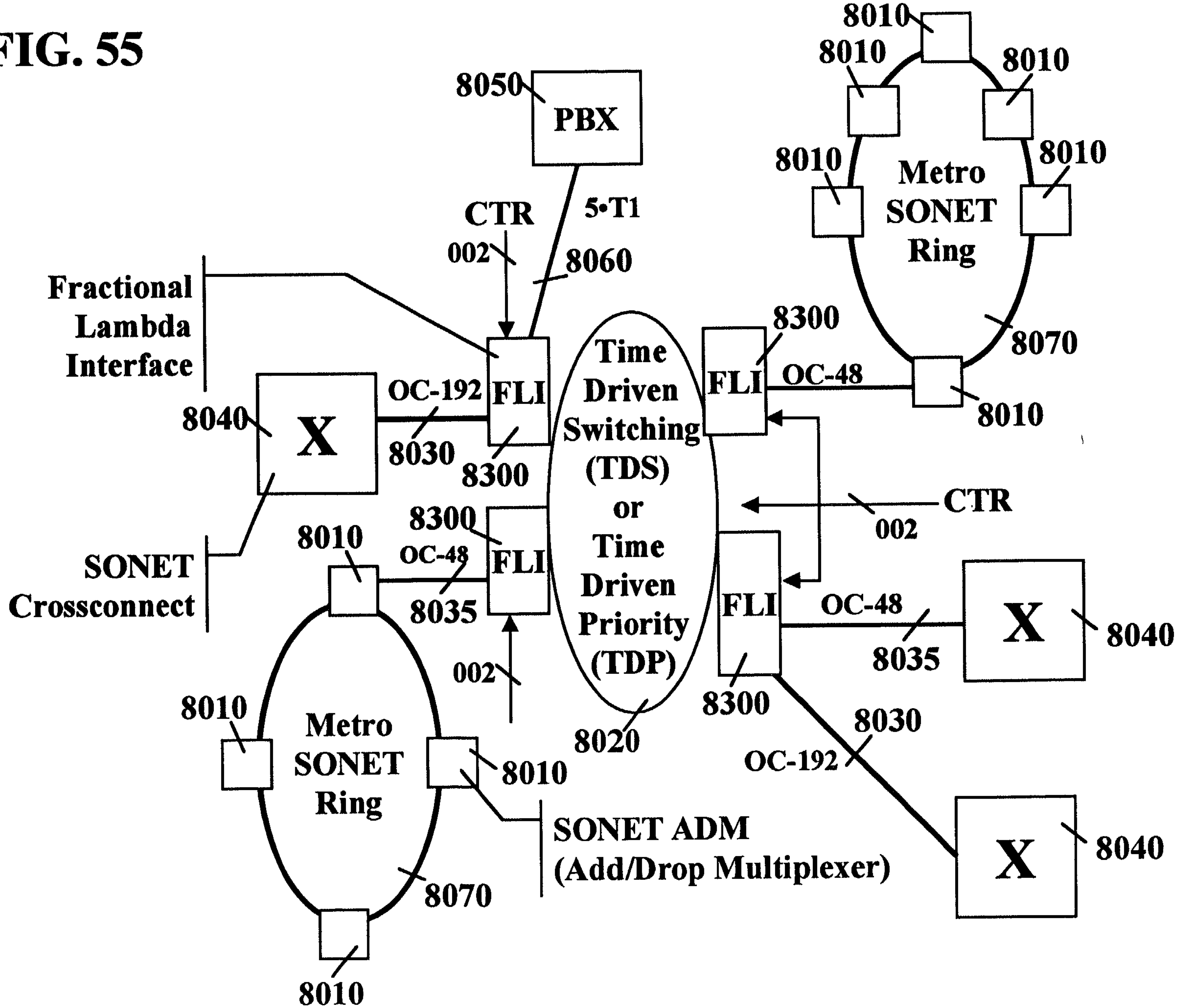

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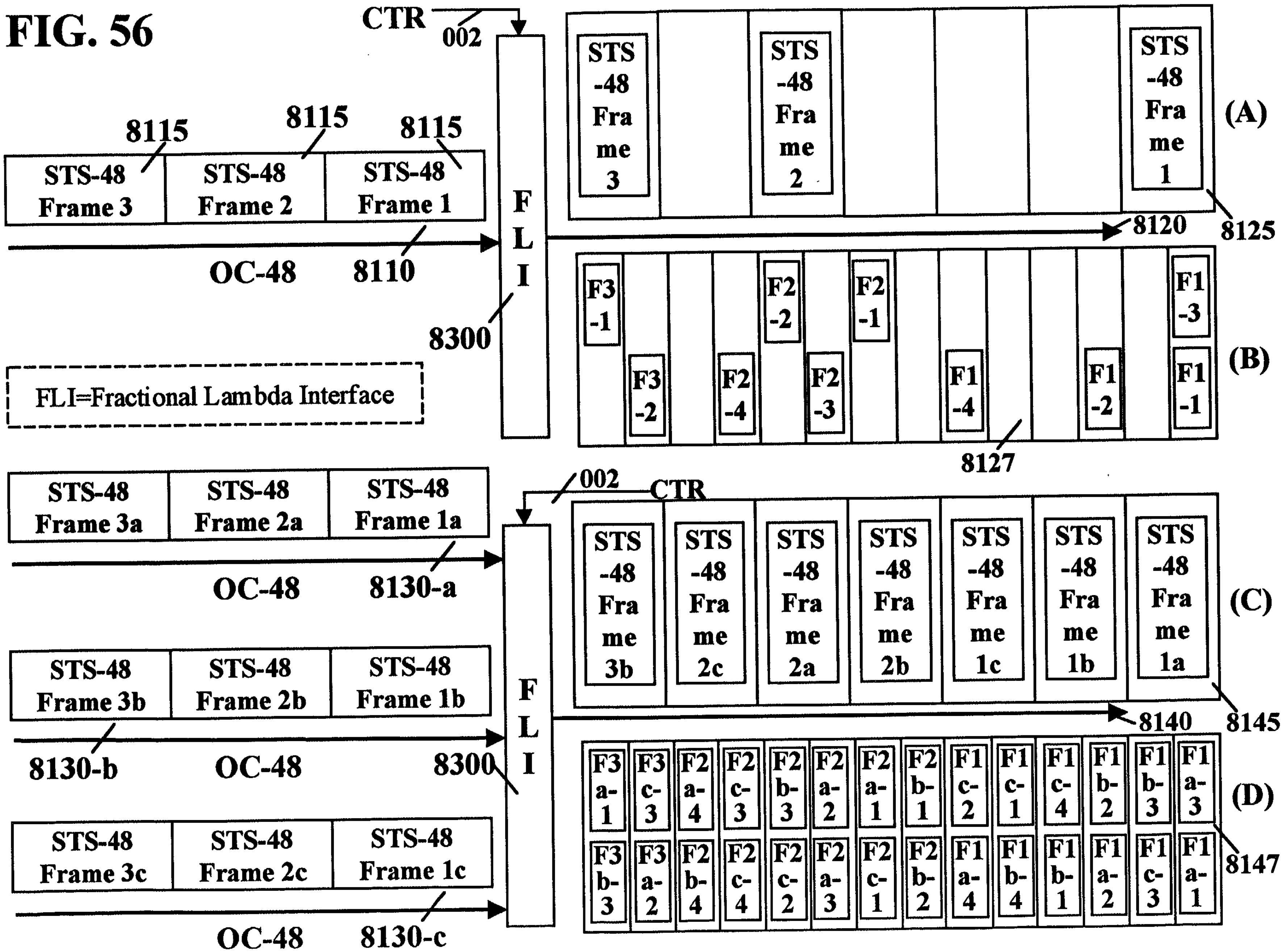
FIG. 56


CTR
002
8115
8115
8115
STS-48 Frame 3
STS-48 Frame 2
STS-48 Frame 1
OC-48
8110
8300
FLI
FLI=Fractional Lambda Interface
STS -48 Frame 3
STS -48 Frame 2
STS -48 Frame 1
(A)
8120
8125
F3 -1
F3 -2
F2 -4
F2 -2
F2 -3
F2 -1
F1 -4
F1 -2
F1 -3
F1 -1
(B)
8127
002
CTR
STS-48 Frame 3a
STS-48 Frame 2a
STS-48 Frame 1a
OC-48
8130-a
STS-48 Frame 3b
STS-48 Frame 2b
STS-48 Frame 1b
8130-b
OC-48
8300
STS-48 Frame 3c
STS-48 Frame 2c
STS-48 Frame 1c
OC-48
8130-c
STS -48 Frame 3b
STS -48 Frame 2c
STS -48 Frame 2a
STS -48 Frame 2b
STS -48 Frame 1c
STS -48 Frame 1b
STS -48 Frame 1a
(C)
8140
8145
F3 a-1
F3 c-3
F2 a-4
F2 c-3
F2 b-3
F2 a-2
F2 a-1
F2 b-1
F1 c-2
F1 c-1
F1 c-4
F1 b-2
F1 b-3
F1 a-3
(D)
F3 b-3
F3 a-2
F2 b-4
F2 c-4
F2 c-2
F2 a-3
F2 c-1
F2 b-2
F1 a-4
F1 b-4
F1 b-1
F1 a-2
F1 c-3
F1 a-1
8147

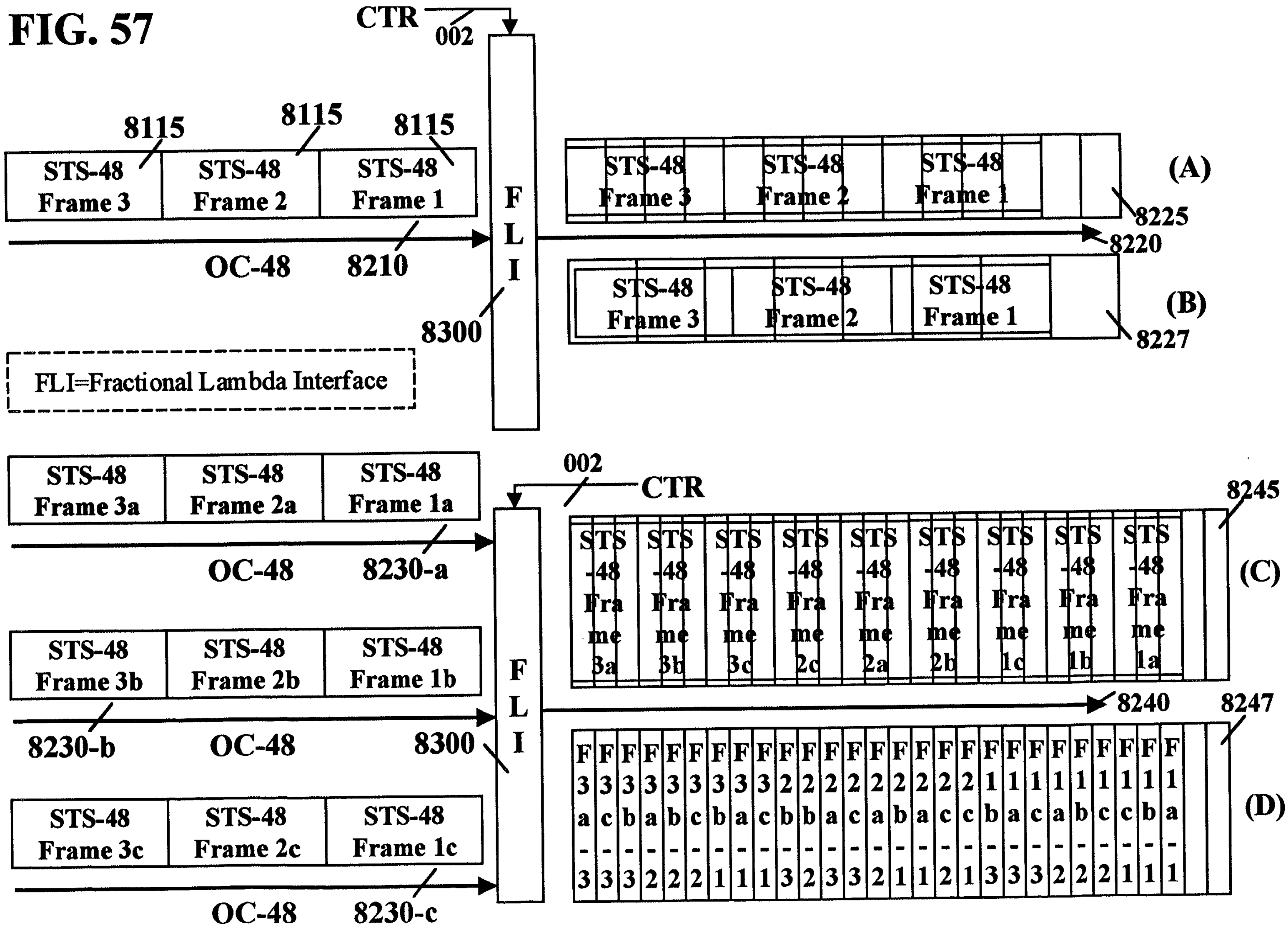
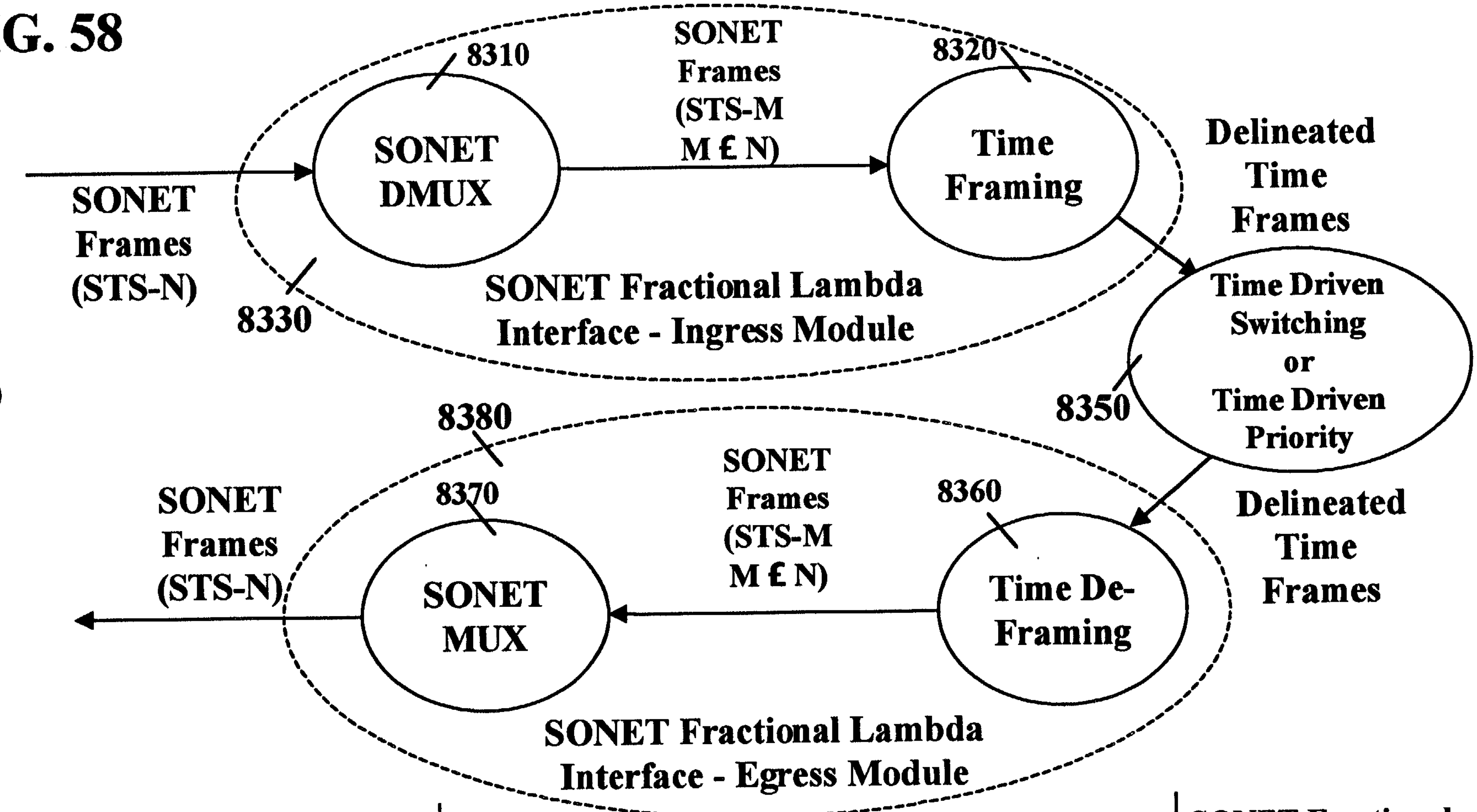

CTR
002
8115
STS-48 Frame 3
STS-48 Frame 2
STS-48 Frame 1
OC-48
8210
F L I
8300
FLI=Fractional Lambda Interface
(A)
8225
8220
(B)
8227
STS-48 Frame 3a
STS-48 Frame 2a
STS-48 Frame 1a
8230-a
STS-48 Frame 3b
STS-48 Frame 2b
STS-48 Frame 1b
8230-b
STS-48 Frame 3c
STS-48 Frame 2c
STS-48 Frame 1c
8230-c
8245
(C)
STS-48 Frame 3a
STS-48 Frame 3b
STS-48 Frame 3c
STS-48 Frame 2c
STS-48 Frame 2a
STS-48 Frame 2b
STS-48 Frame 1c
STS-48 Frame 1b
STS-48 Frame 1a
8240
8247
(D)
F3a-3 F3c-3 F3b-3 F3a-2 F3b-2 F3c-2 F3b-1 F3a-1 F3c-1 F2b-3 F2b-2 F2a-3 F2c-3 F2a-2 F2b-1 F2a-1 F2c-2 F2c-1 F1b-3 F1a-3 F1c-3 F1a-2 F1b-2 F1c-2 F1c-1 F1b-1 F1a-1

FIG. 57

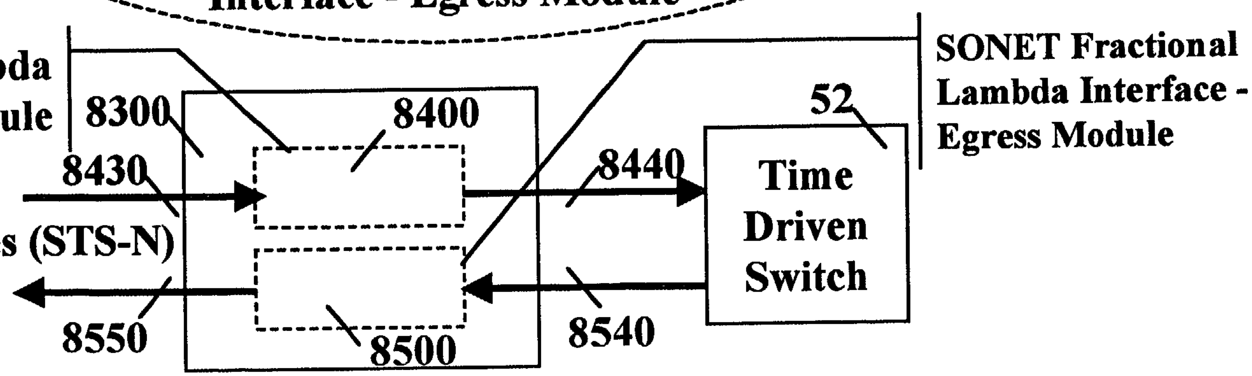
FIG. 58

(A)



SONET Frames (STS-N)
8310
SONET DMUX
SONET Frames (STS-M M £ N)
8320
Time Framing
8330
SONET Fractional Lambda Interface - Ingress Module
Delineated Time Frames
Time Driven Switching or Time Driven Priority
8350
8380
8370
SONET MUX
SONET Frames (STS-M M £ N)
8360
Time De-Framing
Delineated Time Frames
SONET Frames (STS-N)
SONET Fractional Lambda Interface - Egress Module

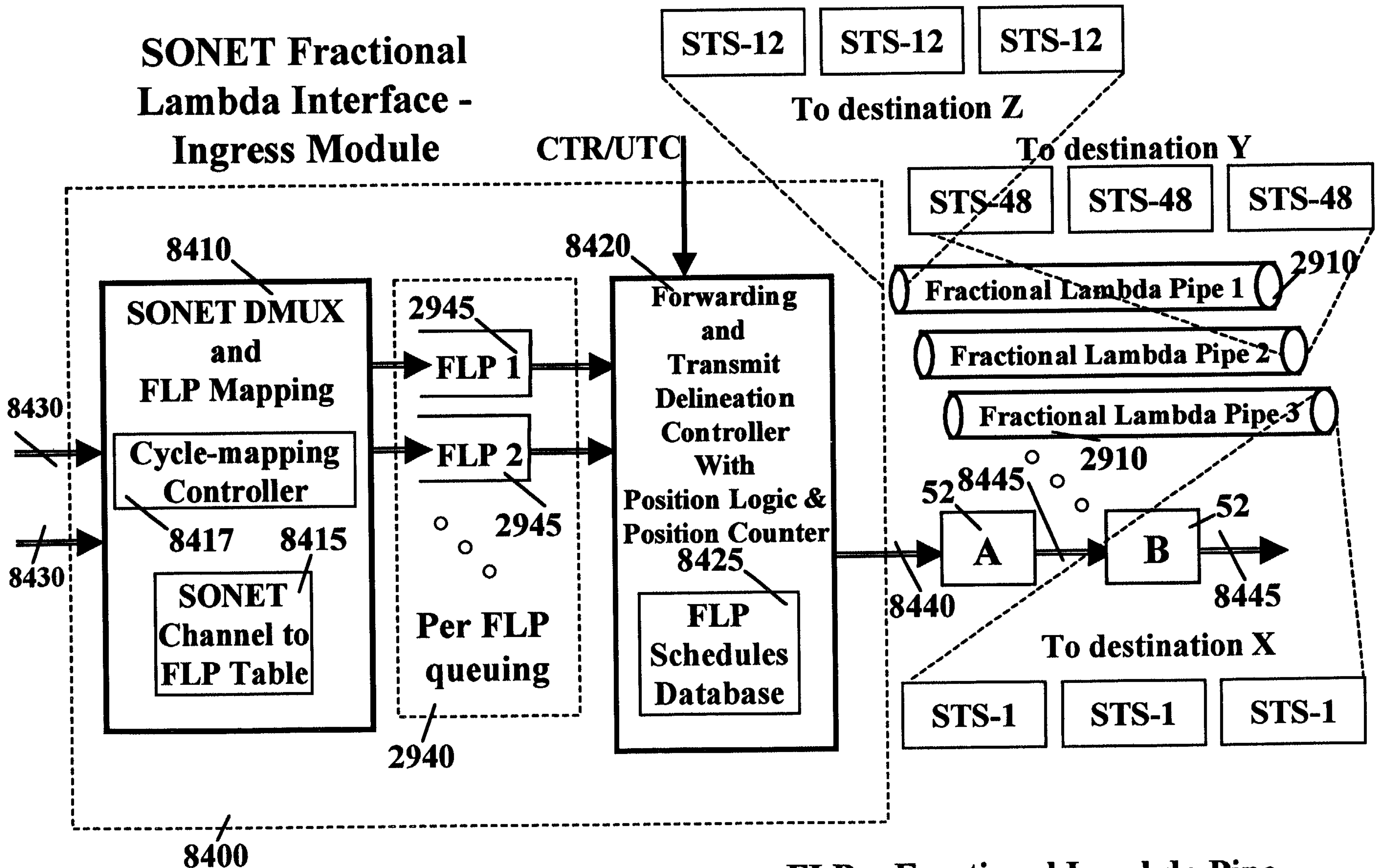
(B)



SONET Fractional Lambda Interface - Ingress Module
8300
8400
8430
8440
SONET Frames (STS-N)
8550
8500
8540
52
Time Driven Switch
SONET Fractional Lambda Interface - Egress Module

FIG. 59

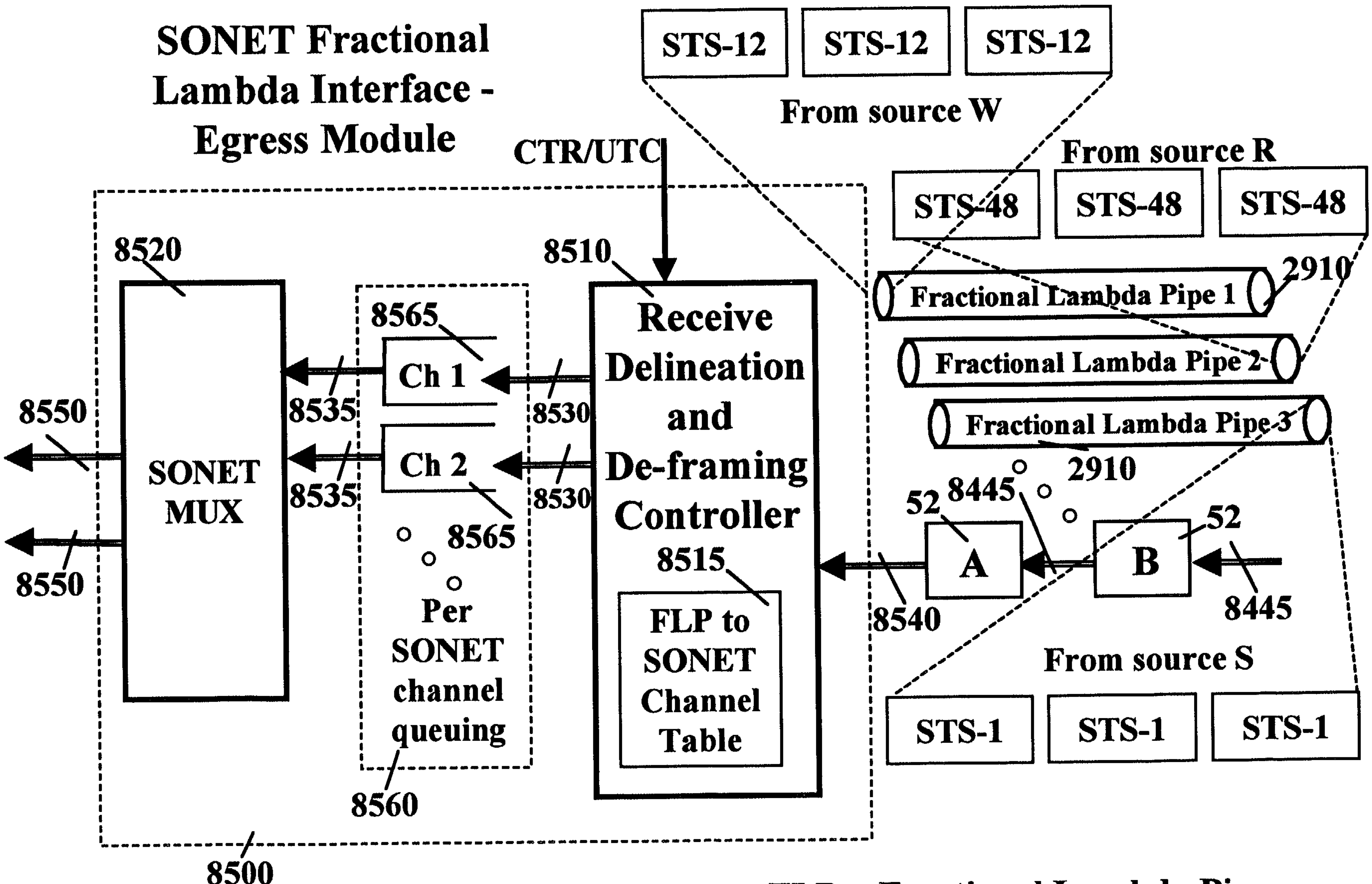
SONET Fractional Lambda Interface - Ingress Module



FLP = Fractional Lambda Pipe

FIG. 60

SONET Fractional Lambda Interface - Egress Module



FLP = Fractional Lambda Pipe

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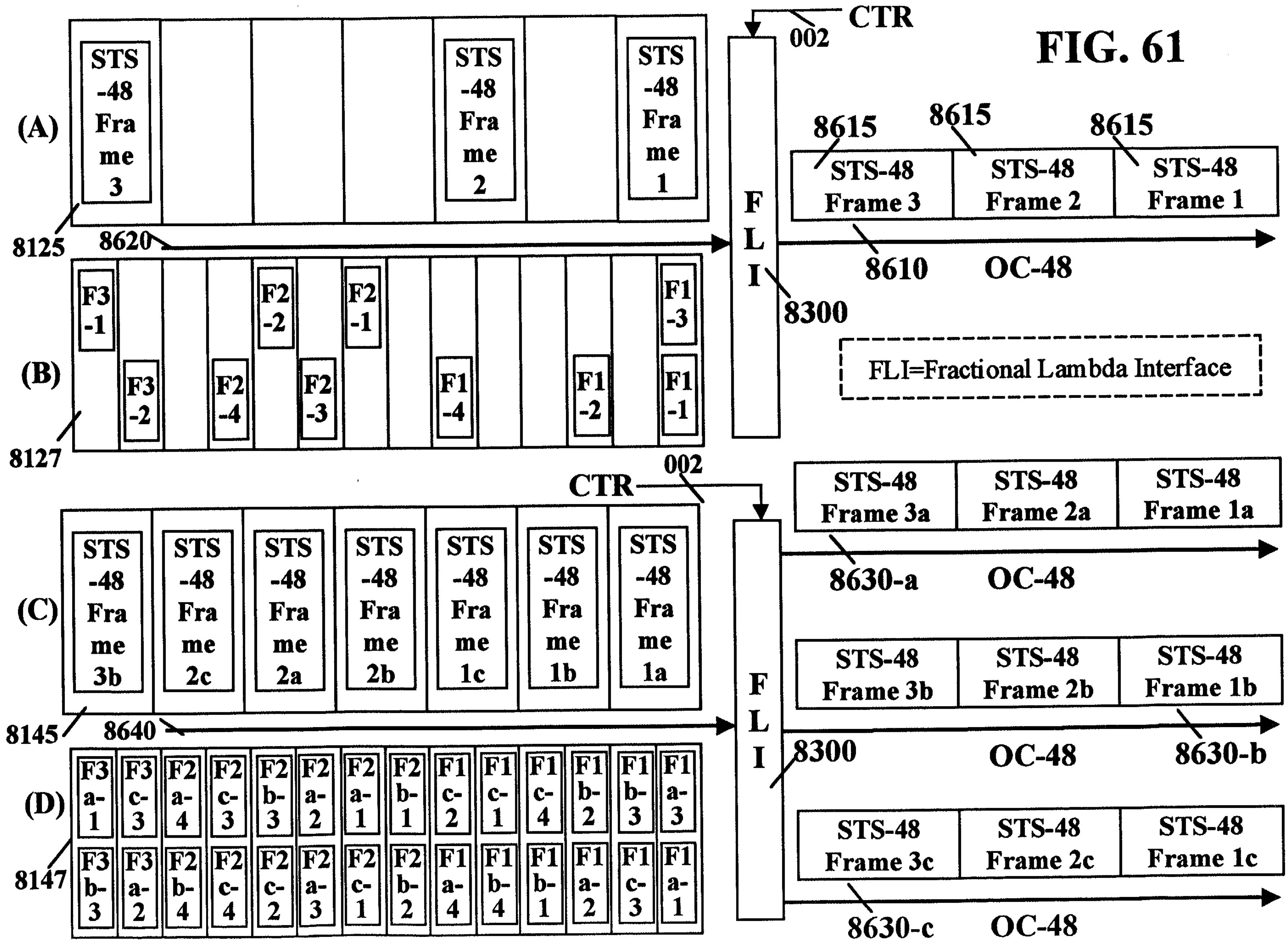
FIG. 61



CTR
002
(A)
STS -48 Frame 3
STS -48 Frame 2
STS -48 Frame 1
8125
8620
(B)
F3 -1
F3 -2
F2 -4
F2 -2
F2 -3
F2 -1
F1 -4
F1 -2
F1 -3
F1 -1
8127
FLI
8300
8615
STS-48 Frame 3
STS-48 Frame 2
STS-48 Frame 1
8610
OC-48
FLI=Fractional Lambda Interface
(C)
STS -48 Frame 3b
STS -48 Frame 2c
STS -48 Frame 2a
STS -48 Frame 2b
STS -48 Frame 1c
STS -48 Frame 1b
STS -48 Frame 1a
8145
8640
(D)
F3 a- 1
F3 c- 3
F2 a- 4
F2 c- 3
F2 b- 3
F2 a- 2
F2 a- 1
F2 b- 1
F1 c- 2
F1 c- 1
F1 c- 4
F1 b- 2
F1 b- 3
F1 a- 3
F3 b- 3
F3 a- 2
F2 b- 4
F2 c- 4
F2 c- 2
F2 a- 3
F2 c- 1
F2 b- 2
F1 a- 4
F1 b- 4
F1 b- 1
F1 a- 2
F1 c- 3
F1 a- 1
8147
STS-48 Frame 3a
STS-48 Frame 2a
STS-48 Frame 1a
8630-a
OC-48
STS-48 Frame 3b
STS-48 Frame 2b
STS-48 Frame 1b
8630-b
STS-48 Frame 3c
STS-48 Frame 2c
STS-48 Frame 1c
8630-c

FIG. 62

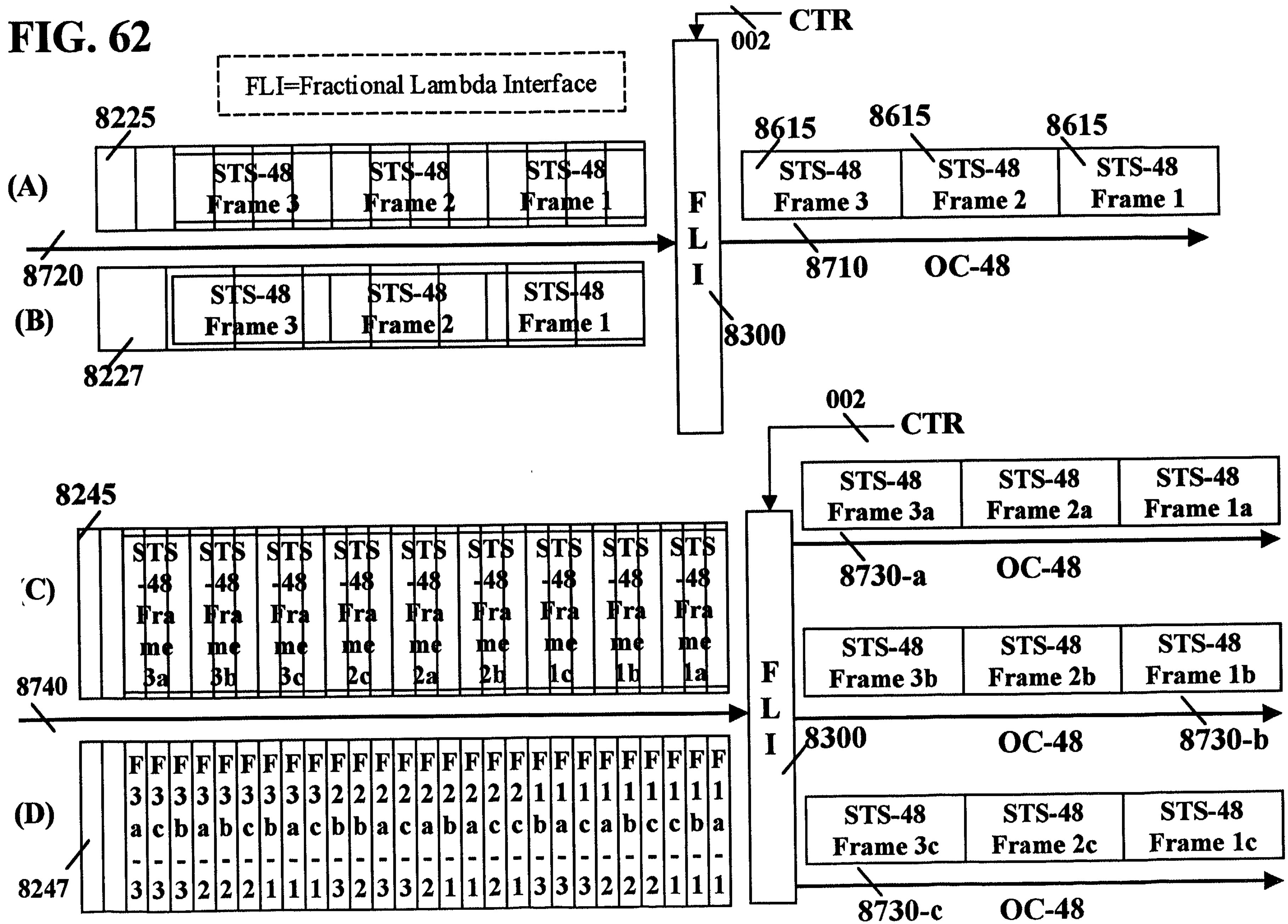

FLI=Fractional Lambda Interface
(A)
8225
STS-48 Frame 3
STS-48 Frame 2
STS-48 Frame 1
8720
(B)
8227
STS-48 Frame 3
STS-48 Frame 2
STS-48 Frame 1
CTR
002
FLI
8300
8615
STS-48 Frame 3
STS-48 Frame 2
STS-48 Frame 1
8710
OC-48
(C)
8245
STS-48 Frame 3a
STS-48 Frame 3b
STS-48 Frame 3c
STS-48 Frame 2c
STS-48 Frame 2a
STS-48 Frame 2b
STS-48 Frame 1c
STS-48 Frame 1b
STS-48 Frame 1a
8740
(D)
8247
F3a-3 F3c-3 F3b-3 F3a-2 F3b-2 F3c-2 F3b-1 F3a-1 F3c-1 F2b-3 F2b-2 F2a-3 F2c-3 F2a-2 F2b-1 F2a-1 F2c-2 F2c-1 F1b-3 F1a-3 F1c-3 F1a-2 F1b-2 F1c-2 F1c-1 F1b-1 F1a-1
CTR
002
FLI
8300
STS-48 Frame 3a
STS-48 Frame 2a
STS-48 Frame 1a
8730-a
OC-48
STS-48 Frame 3b
STS-48 Frame 2b
STS-48 Frame 1b
8730-b
OC-48
STS-48 Frame 3c
STS-48 Frame 2c
STS-48 Frame 1c
8730-c
OC-48

FIG. 63

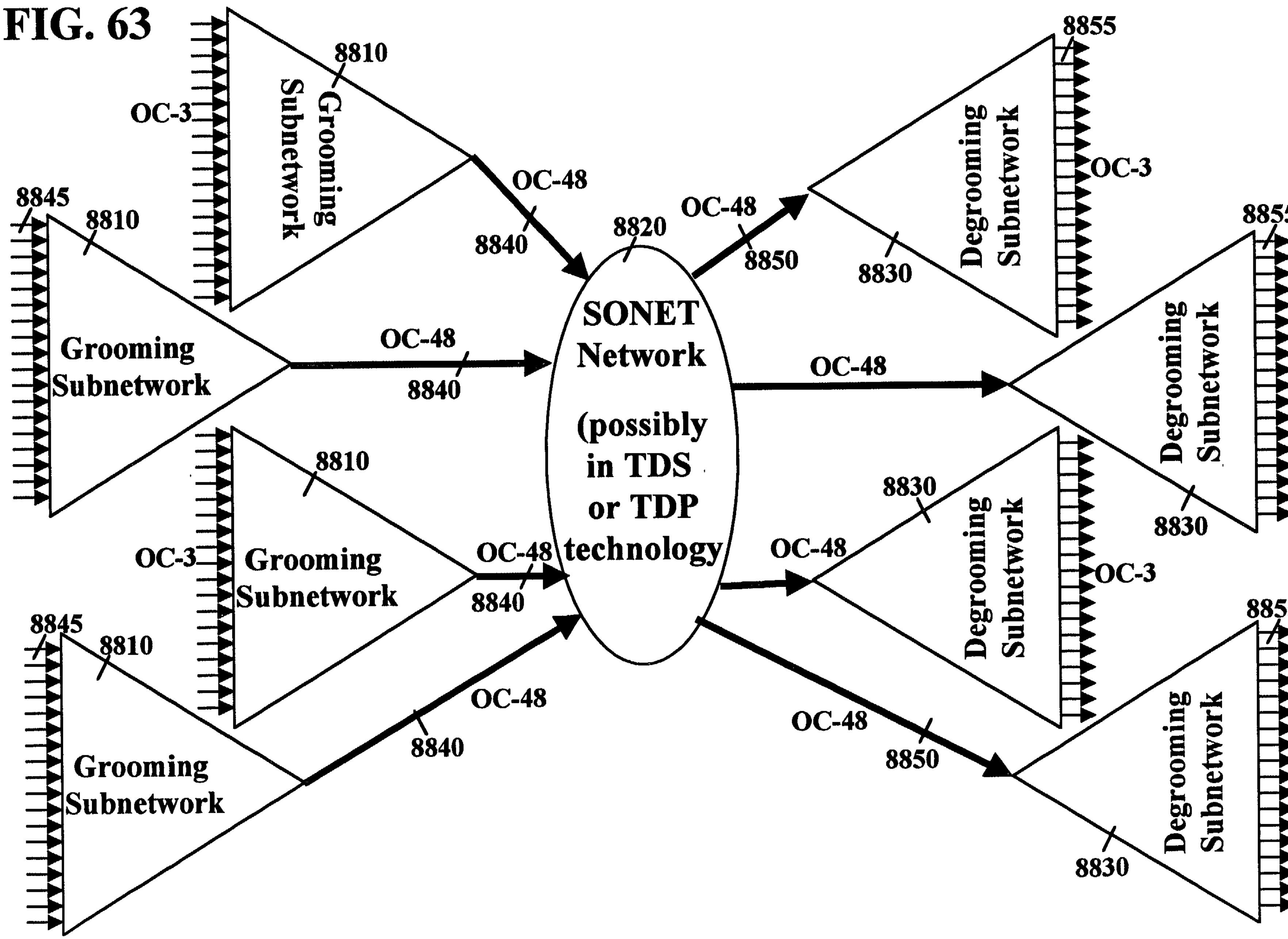

Grooming Subnetwork
Grooming Subnetwork
Grooming Subnetwork
Grooming Subnetwork
8810
8845
OC-3
OC-48
8840
8820
SONET Network
(possibly in TDS or TDP technology)
OC-48
8850
Degrooming Subnetwork
Degrooming Subnetwork
Degrooming Subnetwork
Degrooming Subnetwork
8830
8855
OC-3

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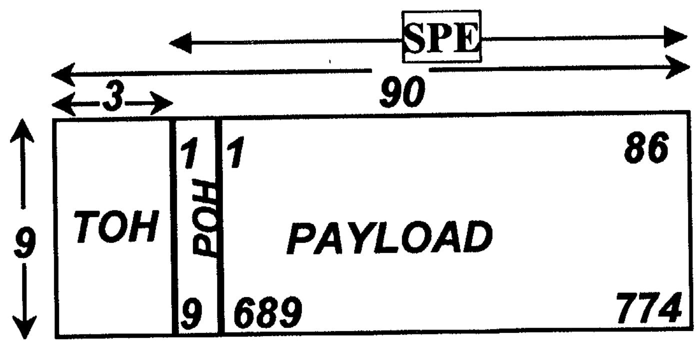
FIG. 64

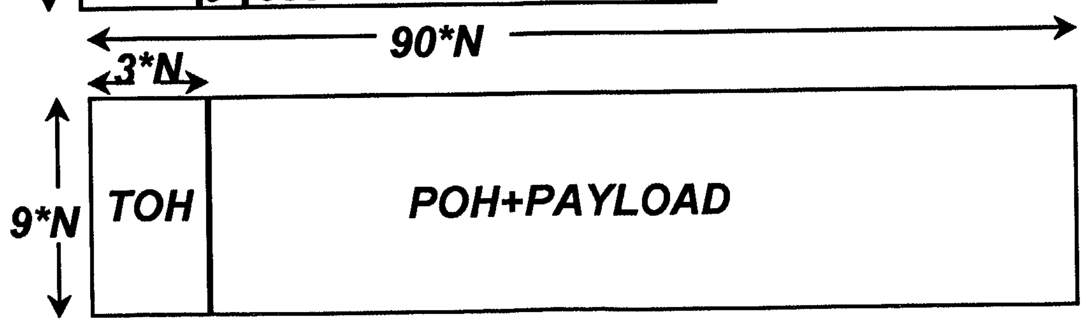
- SONET - synchronous optical network
- Multiplexing method: byte interleaving
- Signal hierarchy: OC-N (STS-N)
  - STS-N rate: N*51.84 Mb/s
  - Frame format: 9 rows by 90*N columns
    - capacity: N*810 bytes in 125 microsecond.
    - overhead: N*27 bytes
    - payload: N*783 bytes

(A)



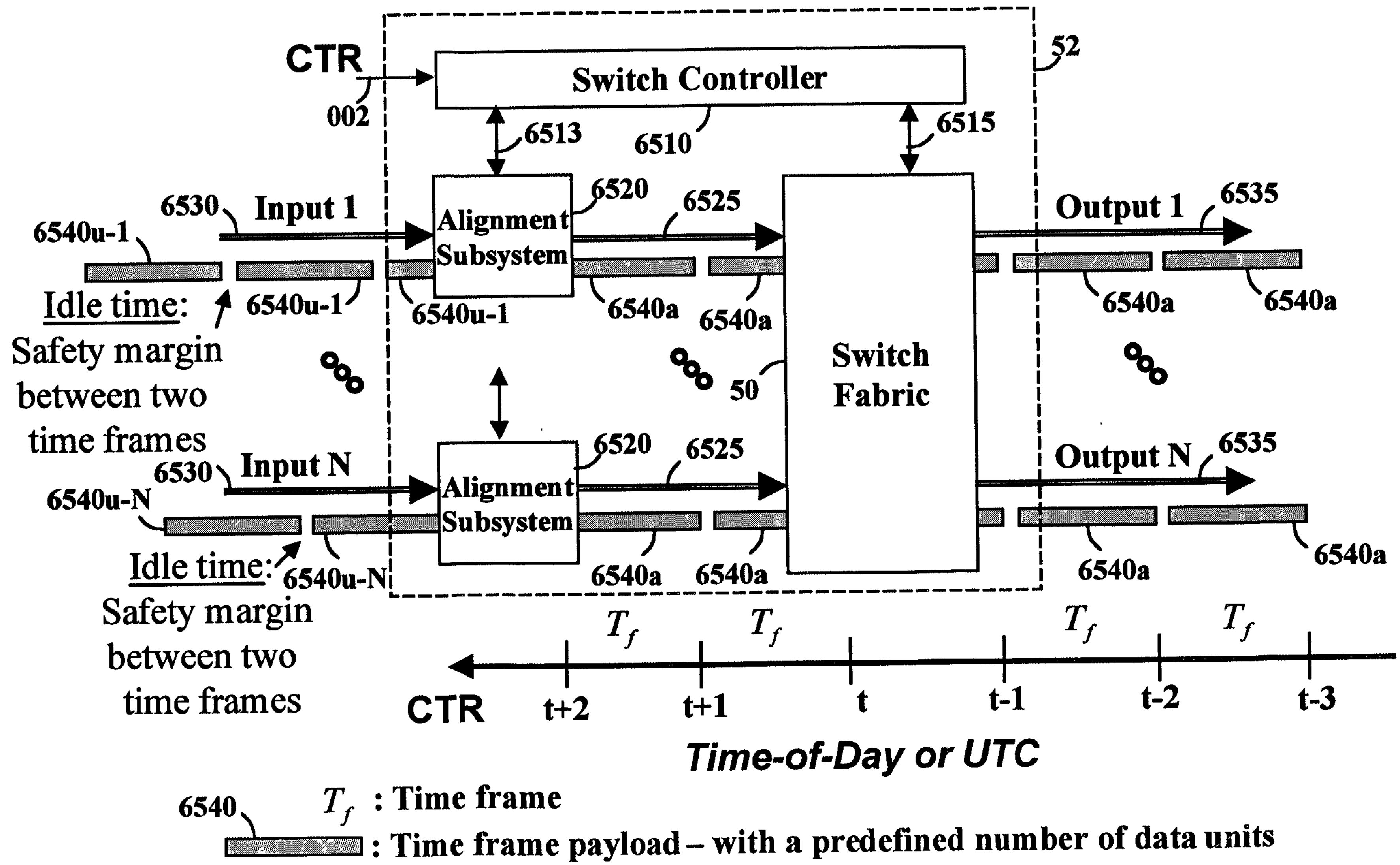
STS-1
SPE - Synchronous Payload Environment
TOH - Transport Overhead
POH - Path Overhead

(B)



STS-N

FIG. 65


CTR
002
Switch Controller
6510
6513
6515
52
6530
Input 1
6540u-1
Idle time:
Safety margin between two time frames
6540u-1
6540u-1
Alignment Subsystem
6520
6525
6540a
6540a
Switch Fabric
50
Output 1
6535
6540a
6540a
6530
Input N
6540u-N
Idle time:
Safety margin between two time frames
6540u-N
Alignment Subsystem
6520
6525
6540a
6540a
Output N
6535
6540a
6540a
T_f
T_f
T_f
T_f
CTR
t+2
t+1
t
t-1
t-2
t-3
Time-of-Day or UTC
6540
T_f : Time frame
: Time frame payload – with a predefined number of data units